

PAPER

Error Identification in At-Speed Scan BIST Environment in the Presence of Circuit and Tester Speed Mismatch

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SUMMARY In this paper, we provide a practical formulation of the problem of identifying all error occurrences and all failed scan cells in at-speed scan based BIST environment. We propose a method that can be used to identify every error when the circuit test frequency is higher than the tester frequency. Our approach requires very little extra hardware for diagnosis and the test application time required to identify errors is a linear function of the frequency ratio between the CUT and the tester.

key words: BIST, fault diagnosis, error identification, at-speed test, low speed tester

1. Introduction

Built-in self-test (BIST) has become the major test technique for today's large scale and high-speed system-on-chip (SoC) designs. Pseudo-random BIST designs are the most widely used due to their relative simplicity and low cost [1]. Since BIST compacts test responses, BIST requires only small tester memory and it can perform at-speed test even if the tester frequency is substantially lower than the frequency of the circuit during test.

On the other hand, BIST causes problems in diagnosis due to its compacted responses. Indeed, pass/fail information obtained from a BIST response analyzer is insufficient for diagnosis. Two kinds of information are required to identify a fault in the CUT. These are 1) the time information (i.e., the input pattern(s) which causes errors), and 2) the space information (i.e., scan cells where errors occur for scan based BIST architecture [1]). Using time information, fault diagnosis can be performed for a given fault model by methods such as dictionary or fault simulation [2]. Using space information, diagnosis can be performed by cone of logic methods [3]. High resolution diagnostic for a given fault model can be achieved by diagnosis techniques combining space information with time information [4], [5].

For scan-based BIST architecture, finding the time when errors occur as the scan chains are unloaded gives both time (failing input pattern) and space (position of erroneous scan cells within the scan chain) information. A number of methods to identify space information have been proposed,

especially for scan-based BIST architectures [6]–[10], however, only a few practical techniques have been developed to identify time information.

Some of the existing techniques are based on signature analysis using cycling register [11] and error correcting codes [12]. These methods compact the complete test response into one signature and can identify certain errors from the signature. Since they observe signature only once, they are suitable even if circuit frequency is much higher than the tester frequency. However, for a large number of error bits, say r errors, they need as many as r -LFSRs or signature registers and may still have over 40% diagnostic aliasing over 40% if the actual number of errors is higher than r [12]. Thus, they either have poor diagnostic resolution or require impractically high hardware overhead to achieve maximum diagnosis resolution. An alternative approach trades off overhead for time by repeating the test sequence and compacting it at each iteration into a different signature [13]. Thus, instead of using r -LFSRs, the test sequence is repeated r times using programmable LFSR to identify r errors. Since it is mathematically equivalent to [12], diagnostic aliasing is the same as using r -LFSRs. Thus, achieving maximum diagnostic resolution requires repeating the test sequence an impractically large number of times.

Techniques that use two phases for diagnosis have also been proposed [14]–[17]. During the first phase, the intermediate signature is checked a few times during test in order to narrow down the failing candidates within some windows. The failing patterns are then identified inside the windows by applying the corresponding patterns one at a time [14] or by using cycling register [15]. These methods use small hardware overhead or test application time. Furthermore, they can be used even if the circuit frequency is higher than the tester frequency. However, occurrence of aliasing may invalidate the result of this diagnosis. Enhancements of these methods have also been studied using variable window size [16], or multiple signature analyzers [17], but they also do not achieve maximum diagnosis resolution.

A commonly used diagnosis technique requires and collects the failing space and time information, without compacting responses, during the diagnosis phase [18]. However, this method requires the circuit to operate at the tester frequency during test. On the other hand, the BIST clock frequency of either capturing or shifting clocks tends to be designed as high as possible to detect timing related

Manuscript received July 21, 2005.

Manuscript revised October 3, 2005.

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DOI: 10.1093/ietisy/e89-d.3.1165

faults and reducing test application time, Therefore, it tends to be higher than the tester frequency. When we slow down the BIST, the faults that affect at-speed operation may not be excited any more and may become un-diagnosable.

In this paper, we propose a method to identify every error occurrence in at-speed scan based BIST environment. Every error can be identified even if the circuit test frequency is higher than the tester frequency. In Sect.2, we formulate the problem of identifying every error occurrence. In Sect.3 we introduce an enhanced procedure to identify every error in at-speed scan BIST environment. In Sect.4, we give an enhanced version of our method and in Sect.5 we show experimental results for a number of circuits including an industrial circuit. Section 6 summarizes the conclusions of our analysis.

2. Problem Formulation

In this section, we formulate the problem of identifying failing response time.

We first identify some characteristics of the diagnosis process and production testing process. Diagnosis can be performed for devices that didn't pass the production test or devices that passed the production test and were found to be faulty in the field. In each case, testing during diagnosis should be performed at the same speed that resulted in the failure of the device.

Another characteristic is that the test application time is not critical for diagnosis. Indeed, typical test application time is at most several seconds, whereas the diagnosis processing on a workstation (such as effect-cause analysis or fault simulation) can take several hours. Hence, the quality of diagnosis is far more important than the test application time.

Our formulation requires the complete diagnosis of a scan based BIST circuit. We assume that BIST operates at-speed during diagnosis. In the at-speed BIST environment, we assume that the CUT operates at frequency f_c , whereas the tester has a frequency limitation and cannot operate at a frequency higher than f_t , such that $f_t < f_c$. The problem is to locate the errors that occur when applying the test set to the circuit. There are two priorities of objectives. The first priority is to maximize the resolution in error location (i.e., identify every error occurrence at frequency f_c) and the second priority is to minimize the test application time. There are two constraints: (1) the CUT should be tested exactly at frequency f_c , and (2) the tester frequency for observation can be no more than f_t .

Finally, the goal of the above methods is to achieve the maximum resolution under the given constraints without increasing tester memory and with little or no hardware overhead. Previous works identified in Sect.1 do not solve this problem. Some of the techniques do not satisfy the conditions imposed on the tester speed, $f_t < f_c$ [18], while others do not achieve the maximum resolution [11],[14]–[17]. Also, most of the known techniques require substantial hardware overhead [12] or test application time [13].

3. Test Application Method for Maximum Diagnostic Resolution

3.1 BIST Architecture and Diagnosis Problem

Figure 1 shows a BIST architecture and its outputs required for diagnosis. The BIST architecture of Fig. 1 is based on the scan-based BIST which is one of the most commonly used architectures. The BIST pattern generator (PG) provides scan inputs, and the signature analyzers (SAs) compact its responses. A MISR is used as signature analyzer during testing, and during diagnosis, a masking circuit allows only one scan chain to feed a SA which is selected by mask select input. As shown in Fig. 1, scan-outs are connected to an output port via a multiplexer during diagnosis like the non-compaction based approach [17]. A Register, FF, is inserted at a scan-out to synchronize tester since CUT test frequency may be higher than the tester frequency.

Erroneous scan chains can be identified using masking circuit. In Fig. 1 for example, by masking scan chains 2 and 4, two SAs compact only scan chains 1 and 3. Similarly, by masking scan chains 1 and 3, two SAs compact only scan chains 2 and 4. We can identify erroneous scan chains by applying k ($=$ No. of scan chains/No of SAs) iterations of BIST patterns.

After erroneous scan chains are identified, we identify failing responses by observing each erroneous scan chain one at a time via a diagnosis output. As shown in [17], we can identify all failing responses by observing scan outputs if CUT test frequency is slower than the tester frequency limitation. However, if CUT test frequency is higher than tester frequency limitation, a tester will not be able to observe every response. Figures 2 and 3 demonstrate this through an example. When the CUT clock period is 3.3 ns and the tester observing period is 10 ns, a tester can observe only 1/3 of the responses. Thus, it will not be able to identify failing responses.

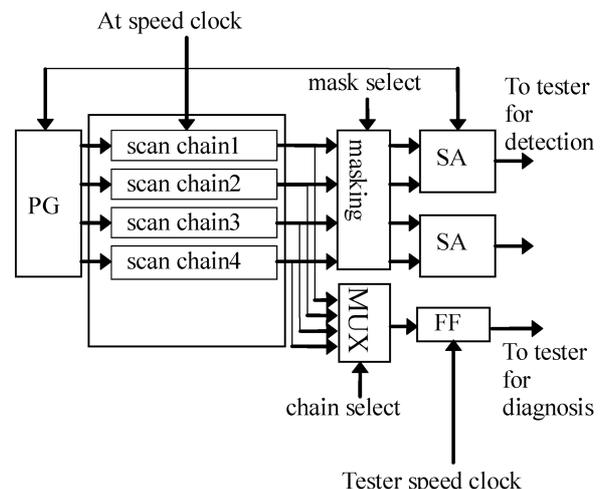


Fig. 1 Diagnosable BIST.

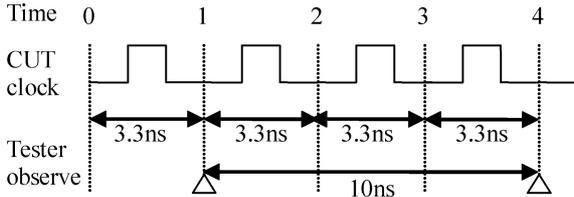


Fig. 2 CUT and observe intervals.

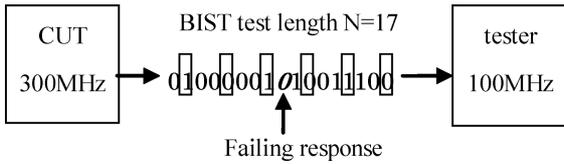


Fig. 3 Scan out and observed results.

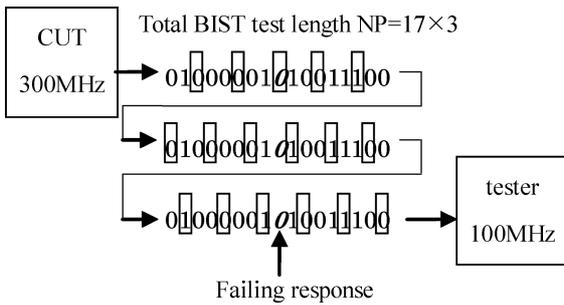


Fig. 4 Successful observation.

The PG, e.g. an LFSR, returns to initial state after generating the last pattern. The initialization can be done without slowing down the test using shadow registers [6]–[8]. If the BIST sequence is 17 cycles long, as shown in Fig. 4, every cycle can be observed by repeating the BIST sequence three times (i.e., applying 51 clocks). During the first sequence, the tester observes response bit 0, 3, . . . , 15. Then bits 1, 4, . . . , 16 are observed during second sequence and bits 2, 5, . . . , 14 during the third sequence. However, such a method may not allow observing all bits in all cases by simple repetition of the sequence. For example if the length of the BIST sequence is 18 the tester can not observe every response by simply repeating the sequence. In the next section, we derive conditions for observing every response bit and describe a method to identify every error occurrence for the above BIST architecture.

3.2 Problem of Observing Every Response

In this paper, we use the following terms.

Absolute time - The number of a scan clock cycle starting from the beginning of the first BIST iteration.

Relative time - The number of a scan clock cycle starting from the beginning of the current BIST iteration.

We use the following notation.

N - Length of the BIST test sequence.

P - Period of the tester relative to the CUT test clock period. We assume that P is an integer and that $1 < P < N$.

R_{min} - Minimum number of BIST iterations to observe every response.

$M(i)$ - Relative time at $(i + 1)^{th}$ observation. The range of $M(i)$ is $0 \leq M(i) < N$

Using the above notation, the method for observing every response can be described as follows.

Observation method: Apply the BIST test sequence of length N R_{min} times, while observing its response at every time period P .

Our goal is to use the above method to observe all the responses to identify every error occurrence. This maximum resolution of an observation is defined as follows.

Definition 1: The response at relative time t ($0 \leq t \leq N-1$) can be observed provided that the equation

$$t = M(x) \tag{1}$$

has a solution x . The maximum resolution can be achieved when all the responses are observed. □

3.3 Conditions to Achieve Maximum Resolution

In this section, we derive the relationship between P and N to achieve the maximum resolution of observation.

Lemma 1: The response at the relative time 1 is observable if and only if P and N are co-prime (i.e., $\gcd(N, P) = 1$).

Proof: $M(i)$ can be expressed as:

$$M(i) = iP \text{ mod } N \tag{2}$$

or,

$$M(i) = iP - kN \tag{3}$$

if the relative time $M(i)$ is observed during the $(k+1)$ th BIST iteration. When the response at relative time 1 is observable, the following equation has a solution.

$$M(i) = 1 \tag{4}$$

or,

$$iP - kN = 1 \tag{5}$$

Equation (5) has a solution (i, k) if and only if P and N are co-prime. □

Lemma 1 shows that $\gcd(N, P) = 1$ is necessary to achieve maximum resolution. Next, we show that it is also sufficient.

Lemma 2: If the number of BIST iterations is no more than P and $\gcd(N, P) = 1$, then the equation

$$M(i) = t \tag{6}$$

cannot have more than one solution.

Proof : If Eq. (6) has two solutions i_1, i_2 , then $M(i)$ can be expressed in two ways by Eq. (3):

$$\begin{aligned} M(i) &= i_1P - k_1N = i_2P - k_2N \\ (i_1 - i_2)P &= (k_1 - k_2)N \end{aligned} \quad (7)$$

Since the number of iterations is smaller than P , we have $0 \leq |k_1 - k_2| < P$. Furthermore P divides $k_1 - k_2$ since P divides $(k_1 - k_2)N$ (from Eq. (7)) and $\gcd(P, N) = 1$. Therefore, $k_1 = k_2$ and $i_1 = i_2$ is deduced. Thus, Eq. (6) cannot have more than one solution. \square

Theorem 1: The maximum resolution is achieved if and only if $\gcd(N, P) = 1$ and the number of BIST iterations is P .

Proof : We assume $\gcd(N, P) = 1$. The number of observations in P BIST iterations is PN/P , i.e., N . Since $M(i)$ for every $0 \leq i < N$ are different by lemma 2, the set $\{M(i): 0 \leq i < N\}$ has to be $\{0, 1, 2, \dots, N-1\}$, i.e., the observing resolution is maximum. Therefore, $\gcd(N, P) = 1$ is a necessary and sufficient condition to achieve the maximum resolution in P iterations. \square

Example 1: Let the length of a BIST sequence be 2^{32} clocks, the CUT test frequency be 500 MHz, and the tester frequency be 100 MHz. In this case the tester observing period is $P = 500/100 = 5$, which is co-prime with 2^{32} , therefore the maximum resolution of observation is achieved.

Example 2: Let the length of a BIST sequence be 2^{10} clocks, the CUT test frequency be 600 MHz, and the tester frequency be 100 MHz. In this case the tester observing period is $P = 600/100 = 6$, which is not co-prime with 2^{10} , therefore the maximum resolution of observation is not achieved.

3.4 Adjusting N or P to Achieve Maximum Resolution of Observation

In Sect. 3.3, we showed that the maximum resolution of observation is always achieved if N and P are co-prime. However, in general, N and P may not be co-prime. In such cases, the maximum resolution of observation can be achieved by adjusting N and/or P . For the problem formulation described in Sect. 2, the following two possibilities exist:

- Increasing the length of BIST sequence N by inserting additional tests or dummy clock cycles.
- Slowing down the tester by increasing tester observation period P .

The adjustment of N and/or P is chosen to minimize the test application time. Let $N' = N + i$ be the adjusted length of the BIST sequence and $P' = P + j$ be the adjusted tester observing period. The test application time is:

$$TAT = \frac{N'P'}{f_c} = \frac{1}{f_c}(NP + iP + jN + ij) \quad (8)$$

The problem is to find a pair (i, j) that minimizes $iP + jN + ij$, with $N + i$ and $P + j$ co-prime.

Theorem 2: If $N \geq P(P - 1)$, the solution (i, j) that minimizes Eq. (8) with $N + i$ and $P + j$ co-prime is such that $j = 0$.

Proof : Since $\gcd(\alpha P + 1, P) = 1$ for any integer $\alpha \geq 0$, there exists a co-prime of P in any consecutive P integers. Therefore, the range of i in Eq. (8) is $0 \leq i < P$. Similarly, the range of j is $0 \leq j < N$. First we consider the case where $j = 0$. The worst case of minimum $iP + jN + ij$ is the case where $i = P - 1$, therefore:

$$iP + jN + ij = (P - 1)P \quad (9)$$

Next, we consider the case when $j \neq 0$. The best case of minimum $iP + jN + ij$ is the case where $i = 0$, therefore:

$$iP + jN + ij = jN \geq N \quad (10)$$

If $N > P(P - 1)$, Eq. (10) is always larger than Eq. (9). Therefore, $j = 0$ is the solution that minimizes Eq. (8). \square

A typical tester can operate at about 50 MHz and the CUT test frequency in modern DSM circuits is increasing to as high as 5 GHz. Thus, we can assume $P < 100$. On the other hand, typical N can be of the order of several millions, making $N > P(P - 1)$. Therefore, in most practical cases it is sufficient to adjust only N by inserting dummy clocks since in such cases $j = 0$ provides the optimal solution.

3.5 Procedure for Identifying Every Error Occurrence

Summarizing Sects. 3.1–3.4, the procedure for identifying every error occurrence using diagnosis outputs is as follows.

Given condition

- Test frequency of CUT: f_c
- Tester frequency limitation: f_t
- Initial BIST test length: N
- Scan cells in a chain: L

Step 1. Set observing time period P as $P = f_c / f_t$.

Step 2. Adjust BIST test length by adding minimum i dummy clocks (i.e., $N' = N + i$) such that N' is co-prime with P .

Step 3. Apply $P \cdot N'$ clocks to BIST pattern generator, observing one scan output every P test cycles.

Step 4. If an error is detected at the $(i + 1)^{th}$ observation, then:

- Relative time of error occurrence e is:
 $e = iP \bmod N'$
- Failing scan pattern = $\lfloor e / (L + 1) \rfloor$
- Erroneous scan cell = $e \bmod (L + 1)$

Note that the scan chain length is incremented by one to identify the failing scan pattern and erroneous scan cell in order to account for the capture cycle between successive scans.

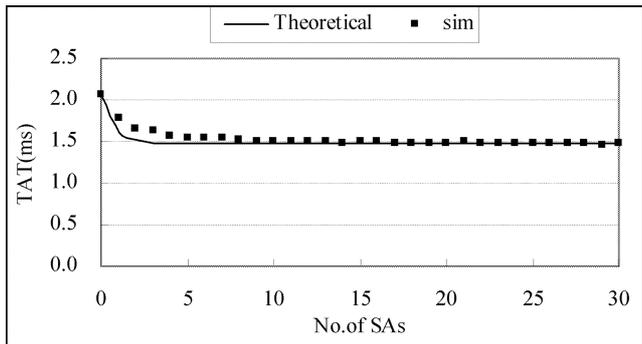


Fig. 7 TAT as a function of number of SAs.

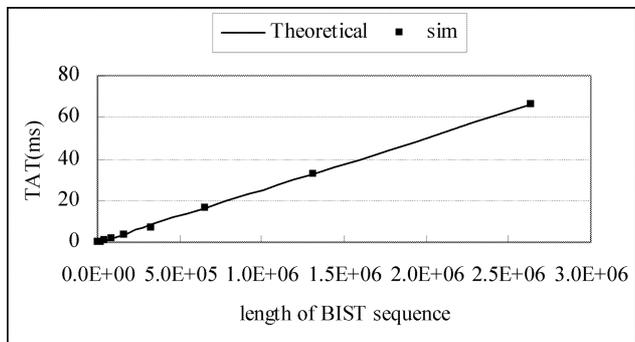


Fig. 8 TAT as a function of BIST sequence length.

time as a function of f_c while keeping $n = 3$ and $N = 82$ K. Figure 7 shows the test application time as a function of n , while keeping $f_c = 3880$ MHz and $N = 82$ K. Finally, Fig. 8 shows the test application time as a function of N while keeping $f_c = 3880$ MHz and $n = 3$.

Clearly more iterations are required as the CUT clock frequency becomes higher relative to the tester frequency. Figure 6 shows that the use of error detectors reduces the test application time for high clock frequency. From Fig. 7 we can conclude that two to three signature analyzers are sufficient as error detectors as no additional reduction in TAT takes place if more SAs are used. Indeed, the test application time is almost constant for more than 3 signature analyzers. Figure 8 shows that the test application time is proportional to the length of BIST sequence. Figures 6–8 collectively also show that the test application time computed by using Eq. (16) is quite close to the simulation results.

Next, we present simulation results for a large industrial circuit. The CUT is a part of a SoC developed at NEC Electronics Co. and we added diagnosable BIST to it for the experiments. Details of the circuit are provided in Table 1. Note that the length of the BIST sequence is the total number of clock cycles including the capture cycle for all the test patterns. We show the results in Table 2 for 20 randomly selected faults. Note that the faults 8 and 11 are not detected by the BIST sequence used in the experiment.

This table shows that errors are observed by only a small number of chains in most cases and error probability is quite different for each fault case. The simulated and

Table 1 Experimental circuit.

No. of gates	6 M gates
No. of FFs	54505
No. of external ports	317
No. of Scan chains	64
No. of SAs	5 (16 bit LFSR)
clock frequency of CUT	1.64 GHz
clock frequency of tester	40 MHz
Length of Test pattern (Length of the BIST sequence)	1000 (54,506,000)

Table 2 Experimental results for industry’s circuit.

fault	Error chain	Pr {1 bit error}	sim skip %	Eq. (15) skip %	sim TAT (ms)	Eq. (16) TAT (ms)
0	1	5.3E-05	31.7	33.4	18.8	18.4
1	1	1.4E-04	4.9	5.8	24.5	24.3
2	1	6.8E-05	26.8	24.3	19.8	20.4
3	7	1.8E-06	85.7	96.2	25.6	9.8
4	1	7.3E-05	19.5	22.0	21.4	20.8
5	1	7.7E-05	24.4	20.0	20.3	21.3
6	3	1.2E-06	87.0	97.6	12.5	5.7
7	1	1.4E-04	2.4	5.0	25.0	24.5
8	0	0	—	—	—	—
9	6	1.4E-06	86.6	97.2	21.4	7.8
10	51	1.1E-05	76.5	80.1	260.7	220.8
11	0	0	—	—	—	—
12	1	5.8E-04	0.0	0.0	25.6	25.5
13	1	6.8E-05	24.4	24.3	20.3	20.4
14	3	5.8E-06	82.9	88.5	15.1	11.5
15	1	1.2E-04	4.9	8.1	24.5	23.8
16	1	1.9E-05	68.3	67.7	11.0	11.1
17	1	5.8E-04	0.0	0.0	25.6	25.5
18	1	9.8E-05	12.2	12.9	22.9	22.8
19	1	1.4E-04	0.0	5.0	25.6	24.5

theoretical skip ratio ($E(skip)/P$) and test application time are also shown in Table 2. Once again we observe a close match between the real simulation data and the results of our theoretical expression (Eqs. (15) and (16)). We also notice from Table 2 that the TAT for identifying all erroneous scan chains in case 10 is substantially larger than in the other cases. This is because the number of erroneous scan chains for this case is very large. None the less total TAT for case 10 is still within 1 second, which is quite practical for diagnosis. Longer BIST sequence may be needed to detect faults 8 and 11; we expect the TAT to be proportional to the length of the BIST sequence as described in the first experiment.

6. Conclusions

In this paper, we proposed a method for identifying every failing pattern and all erroneous scan cells for the BIST architecture. Our approach is efficient even if the CUT test clock frequency is much higher than the tester frequency. Tester can observe every response in the limited number of BIST iterations determined by the ratio of CUT clock frequency and the tester frequency.

We also proposed a method to use signature analyzers as error detectors to reduce the number of BIST iterations.

Experimental results show that the error detectors can reduce the number of BIST iterations by more than 10% when large number of iterations is required. Experimental results show that two or three signature analyzers are sufficient as error detectors. Therefore, our approach achieves the maximum resolution with very low hardware overhead in practical test application time.

Acknowledgments

This work was supported in part by 21st Century COE Program and in part by Japan Society for the Promotion of Science (JSPS) under Grants-in-Aid for Scientific Research B(2)(No.15300018) and the grant of JSPS Research Fellowship (No.L04509). The authors would like to thank Prof. Michiko Inoue, Prof. Satoshi Ohtake, Prof. Tomokazu Yoneda and members of the Fujiwara Laboratory for providing valuable comments throughout this research.

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