

PAPER

Analysis of Test Generation Complexity for Stuck-At and Path Delay Faults Based on τ^k -Notation

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SUMMARY In this paper, we discuss the relationship between the test generation complexity for path delay faults (PDFs) and that for stuck-at faults (SAFs) in combinational and sequential circuits using the recently introduced τ^k -notation. On the other hand, we also introduce a class of cyclic sequential circuits that are easily testable, namely two-column distributive state-shiftable finite state machine realizations (2CD-SSFMS). Then, we discuss the relevant conjectures and unsolved problems related to the test generation for sequential circuits with PDFs under different clock schemes and test generation models.

key words: *easily testable, stuck-at faults, path delay faults, test generation complexity*

1. Introduction

The τ^k -notation was introduced to express the test generation complexity of several classes of sequential circuits with respect to the test generation complexity for stuck-at faults (SAFs) in combinational circuits, which is named τ [1], [2]. The empirical observation showed that the test generation complexity for practically encountered combinational circuits with single SAFs seems to be polynomial. Therefore, the τ^k -notation allows classifying test generation problems as easy or hard, although theoretically, they are proved NP-complete. Our work consists of deriving the test generation complexity for well-known classes of circuits and defining new classes of circuits that can be considered easy to test.

An acyclic sequential circuit is a sequential circuit without feedback. An acyclic sequential circuit is said to be a *balanced sequential circuit* [4] if, for any pair of primary input and primary output, all paths between them have the same number of flip-flops while it is an *internally-balanced sequential circuit* [3] if a circuit resulting from operation 1 of the extended combinational transformation in [3] on an acyclic sequential circuit is a balanced sequential circuit. The test generation for internally balanced sequential circuits and balanced sequential circuits with SAFs has been shown to be reducible into that for combinational circuits with SAFs [3], [4]. Furthermore, the test generation complexity for acyclic sequential circuits with SAFs has been proved to be bounded by the square of the combinational test generation for single SAFs in [1], [2]. Apart from

SAF, which is representative of static faults, path delay fault (PDF) model need to be considered to ensure the temporal correctness of a circuit. As a first step, we only consider robust and non-robust faults in this paper. Previous works [5]–[7], [9] have shown that the combinational automatic test pattern generation (ATPG) tool for SAFs, together with some circuit transformations can be used as an ATPG for robust and non-robust path delay faults. However, the test generation was not discussed explicitly in the aspect of time complexity. Neither was the test generation complexity for sequential circuits with PDFs.

In this paper, we analyze the test generation complexity for combinational circuits with robust and non-robust PDFs, which is shown equivalent to the test generation for combinational circuit with SAFs. Furthermore, we analyze the test generation complexity for sequential circuits including cyclic sequential circuits with SAFs and PDFs. The study conducted in this paper leads to two applications. First, based on the properties of a known class, a special ATPG can be designed to run the test generation for the circuit more efficiently than a general sequential ATPG. Another application is design for testability (DFT) and synthesis for testability (SFT). For a given arbitrary sequential circuit (resp. arbitrary design), a DFT method (resp. SFT method) can be designed and applied to augment the circuit into one of the easily testable classes of sequential circuits identified in this paper.

After determining the test generation complexity for each class of circuits with SAFs and PDFs, we compare the test generation complexity for SAFs and that for PDFs. Our interest is whether there exists any class of circuits for which the test generation complexities with SAFs and PDFs are not equivalent. If there exists such a class of circuits, the following question arises. “Which complexity is higher, the one for SAFs or PDFs?” We present a class of sequential circuits named two-column distributive SSFSM realizations for which the test generation for SAFs and that for PDFs might not be equivalent.

The organization of the paper is as follows. In Sect. 2, we present the τ^k -notation. In Sect. 3, we reconsider the test generation complexity for combinational circuits with robust and non-robust PDFs. We also consider the test generation complexity for combinational circuits with robust and non-robust segment delay faults (SDFs) in Sect. 4 as the result is useful in analyzing the test generation complexity for sequential circuits with PDFs. In Sect. 5, we discuss the test generation complexity for acyclic sequential circuits with

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path delay faults. This is followed by the discussion of the test generation complexity for a class of cyclic sequential circuits called 2CD-SSFMS with SAFs and PDFs in Sect. 6. Conclusion is presented in the final section.

2. Preliminaries

The definition of τ^k -notation [1], [2] is presented briefly in this section. Let $g(n)$ be a given function. The following describes briefly $\Theta(g(n))$ and $O(g(n))$. A function $f(n)$ belongs to the set $\Theta(g(n))$ if $g(n)$ is an asymptotically tight bound for $f(n)$. A function $f(n)$ belongs to the set $O(g(n))$ if $g(n)$ is an asymptotically upper bound for $f(n)$. Empirical observation of combinational test generation complexity for SAFs allows us to use the following assumption on the test generation complexity in our discussion.

Assumption: The test generation complexity for a combinational circuit with SAFs is $\Theta(n^r)$ for some r larger than 2, where n is the number of gates in the combinational circuit.

In the following text, the term “size” will be used in place of “number of gates” since the term is more common in the discussion of time complexity. All gates are regarded as primitive gates. By denoting $\Theta(n^r)$ as $\tau(n)$, the τ^k -notation is defined as follows.

Definition 1: Let $T(n)$ denote a time complexity. $T(n)$ is τ^k -*equivalent* if and only if $T(n) = \Theta(\tau^k(n))$ and τ^k -*bounded* if and only if $T(n) = O(\tau^k(n))$, where $k > 0$.

3. Combinational Circuits with Path Delay Faults

In this section, we define a single-path leaf-dag C_P^{LD} for path P and a path rising-smooth circuit C_P^{RS} for path P , which are the pseudo circuits transformed from a given combinational circuit prior to test generation, based on [5]. These transformations allow us to generate tests for a PDF on P in the given combinational circuit by running ATPG on the pseudo circuits with the corresponding SAF. The complete proofs for all lemmas and theorems in this section can be found in [13].

Definition 2: A *single-path leaf-dag* C_P^{LD} for path P is a combinational circuit such that a fanout and an inverter along P are only permitted at the starting point of P and the output of the inverter, if one exists along P , is not allowed to have fanouts.

Definition 3: Let P denote a path in a given combinational circuit C . C can be transformed into a single-path leaf-dag C_P^{LD} for path P , by the *single-path-leaf-transformation*:

- S1. P consists of an ordered set of gates $\{g_1, g_2, \dots, g_m\}$, where g_1 is a primary input and g_m is a primary output. Also, gate g_j is an input to gate g_{j+1} ($1 \leq j \leq m - 1$). Let $Pre(g_j)$ denote a set of predecessor gates $\{g_1, g_2, \dots, g_{j-1}\}$ on P . Traversing from g_m , if a gate g_j has a fanout of two or more, each gate in $Pre(g_j)$ with the connections to its immediate predecessor gates

are duplicated once. Let g'_k denote the duplicate of g_k , where $g_k \in Pre(g_j)$. For each g_k in $Pre(g_j)$ and for each immediate successor gate h_{k+1} of g_k which is not on P , the connection of g_k to h_{k+1} is changed to the connection of g'_k to h_{k+1} . The resulting path P is free of fanout.

- S2. Starting from g_m along P , all the NAND (resp. NOR) gates on P are changed to the OR (resp. AND) gates using De Morgan’s Law.

The size of the transformed circuit is at most $2n$ where n is the size of C [13].

Definition 4: The *I-edge* of path P with input i in a single-path leaf-dag C_P^{LD} refers to the first connection of P after the inverter, if it exists. The I-edge is said to be associated with input i .

Let i denote a primary input on a path P , the I-edge of P and other fanout branches of i have a transition if i has a transition. The transition from a fanout branch of i may propagate to the side-input of a gate on P . Using I-edge as one of the properties, the pseudo-circuit called path rising-smooth circuit C_P^{RS} (resp. path falling-smooth circuit C_P^{FS}) is introduced.

Definition 5: A single-path leaf-dag C_P^{LD} for path P can be transformed into a *path rising-smooth circuit* C_P^{RS} (resp. *path falling-smooth circuit* C_P^{FS}) for path P by the *path rising-smooth (resp. path falling-smooth) transformation*:

- S1. Let Q_{OR} (resp. Q_{AND}) denote the OR gates (resp. AND gates) along P that have a rising (resp. falling) transition along. A gate may have no parity, 0, 1 or both parities. A gate fed to the side-input of an OR gate (resp. AND gate) in Q_{OR} (resp. Q_{AND}) has parity 1 (resp. 0). Perform a reverse topological traversal of the gates Q in the transitive fanout of i , to determine the parity of all gates along the side-paths to P where i is the primary input on P . The parity is complemented across a NOT gate. If some fanouts of a gate have parity 1 and others have parity 0, the gate is assigned both parities.
- S2 Duplicate the gates so that the parity of each resulting gate is either nothing, 0, or 1, but not both, depending on its successor gates.
 - S2.1 Traversing from the primary output g_m on P , for each gate h_j with a parity (parities) and with a successor gate that is off path and without parity, h_j and the connections to its immediate predecessor gates are duplicated once and its duplicate h'_j has no parity. For each immediate successor gate h_{j+1} of h_j that is off path and has no parity, the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1} .
 - S2.2 Traversing from the primary output g_m on P , each gate h_j with both parities is duplicated along with its connections to its immediate predecessor gates and assigned parity 1. Its duplicate h'_j is assigned parity 0. For each immediate successor gate h_{j+1}

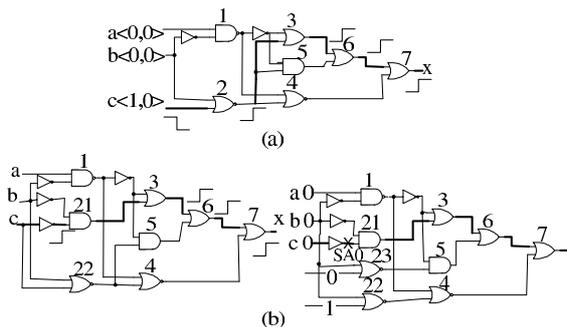


Fig. 1 (a) A circuit with PDF $c2367x \uparrow$. (b) Its single-path leaf-dag (left) and its path rising-smooth circuit (right).

of h_j that has parity 0 (1 if there is an inversion between h_j and h_{j+1}), the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1} .

- S3. Let input i denote the primary input on P . Assign 0 to any fanout branch of input i (or the first connection after the inverter, if it exists on the fanout branch) that is connected to a gate with parity 0 and 1 to any fanout branch of input i (or the first connection after the inverter, if it exists on the fanout branch) that is connected to a gate with parity 1.

The size of the resulting circuit is at most $2n$ where n is the size of the circuit before transformation [13].

The parity at the fanout branch of i , which is not its I-edge, is the constraint that makes sure the generated tests does not propagate a transition from the fanout branch to the side input of a gate on path P .

Figure 1 shows a combinational circuit and its single-path leaf-dag and path rising-smooth circuit for path $c2367x$. In order to analyze the test generation complexity for PDFs, we now derive some results regarding the complexity for the single-path-leaf transformation and the path rising-smooth transformation. In the following text, $P \uparrow$ (resp. $P \downarrow$) denotes a rising (resp. falling) PDF where the rising (resp. falling) transition refers to the transition type at the starting point of P .

Lemma 1: Let C denote a given combinational circuit with size n . The time complexity of the single-path-leaf transformation on C with $P \uparrow$ (resp. $P \downarrow$) is $O(n^2)$.

Lemma 2: Let C denote a single-path leaf-dag with size n and $P \uparrow$ (resp. $P \downarrow$) denote a rising (resp. falling) PDF. The time complexity of the path rising-smooth (resp. path falling-smooth) transformation on C with $P \uparrow$ (resp. $P \downarrow$) is $O(n^2)$.

Definition 6: A vector pair $\langle \tilde{v}, v \rangle$ is a *single-input-change (SIC) two-pattern test* if there exists a coordinate i such that $\tilde{v}_i = \bar{v}_i$ for the coordinate i of v and $\tilde{v}_j = v_j$ for each coordinate j other than i .

In robust PDF test generation using combinational ATPG, the second pattern of a two-pattern test is first generated. Then, the first pattern is derived from the second

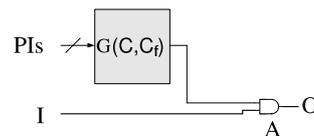


Fig. 2 A circuit C_f^δ .

pattern. Therefore, we are interested in the time complexity to obtain an SIC two-pattern test.

Lemma 3: The time complexity of single-input-change (SIC) two-pattern n -bit test transformation is $O(n)$.

Definition 7: A given combinational circuit C with a SAF f can be transformed into a circuit C_f^δ (Fig. 2) by the δ transformation as follows:

- S1. Let o_1, \dots, o_p denote the primary outputs of C . Let c_1, \dots, c_p denote the XOR function of each primary output of C and the corresponding primary output of the faulty circuit C_f . Let $G(C, C_f)$ be the circuit realizing $c_1 \text{ OR } \dots \text{ OR } c_p$.
- S2. Connect the output of $G(C, C_f)$ to a two-input AND gate A . The other input of the AND gate A is a primary input I while the output of the AND gate A is a primary output O in C_f^δ .

Lemma 4: Let $P = \{I, A, O\}$. Let C and C_f^δ denote a combinational circuit and its δ -transformed circuit, respectively. v is a test for a SAF f in C if and only if $\langle v \sim 0, v \sim 1 \rangle$ (resp. $\langle v \sim 1, v \sim 0 \rangle$) is a robust test for path $IAO \uparrow$ (resp. $IAO \downarrow$) in the corresponding circuit C_f^δ where $v \sim b$ denotes the concatenation of vector v and bit b that is a value at the primary input of P .

Lemma 5: The test generation complexity for combinational circuits with SAFs at primary inputs is τ -equivalent.

Now that we have defined and analyzed the transformations used to show the relationship between the test generation for PDFs and the test generation for SAFs, we derive the theorems relating test generation complexity for combinational circuits with robust PDFs and with SAFs.

Lemma 6: $\langle v_1, v_2 \rangle$ is a robust test for the $P \uparrow$ (resp. $P \downarrow$) in the path rising-smooth-circuit C_P^{RS} for P , if and only if $\langle v_1, v_2 \rangle$ is a robust test for the $P \uparrow$ (resp. $P \downarrow$) in the single-path leaf-dag C_P^{LD} for P .

Lemma 7: v is a test for the SA0 (resp. SA1) fault at the I-edge of P in the C_P^{RS} for path P if and only if the SIC vector pair $\langle \tilde{v}, v \rangle$ is a robust test for the $P \uparrow$ ($P \downarrow$) in C_P^{LD} .

Theorem 1: The test generation complexity for combinational circuits with robust PDFs is equivalent to the test generation complexity for combinational circuits with SAFs, i.e. it is τ -equivalent.

Sketch of proof: Lemmas 6 and 7 have proved the equivalence between the test generation for combinational circuits with robust PDFs and the test generation for path rising-smooth circuits with SAFs at I-edges, which is τ -bounded.

On the other hand, Lemmas 1-3 prove that the test generation for combinational circuits with robust PDFs is reducible to the test generation for path rising-smooth circuits with SAFs at I-edges in time $O(n^2)$. Assume the test generation for combinational circuits with robust PDFs is not τ -equivalent, then by using transformation δ , the test generation for combinational circuits with SAFs is not τ -equivalent from Lemmas 4 and 5 either, which is a contradiction. *q.e.d.* Analogous to the test generation problem for combinational circuits with robust PDFs, by considering single-path leaf-dags instead of path rising-smooth circuits, we have the following theorem.

Theorem 2: The test generation complexity for combinational circuits with non-robust PDFs is equivalent to the test generation complexity for combinational circuits with SAFs, i.e. it is τ -equivalent.

Theorems 1 and 2 show that the combinational test generation complexity for robust and non-robust PDFs is τ -equivalent.

4. Combinational Circuits with Segment Delay Faults

In this section, we evaluate the test generation complexity for combinational circuits with segment delay faults (SDFs). The complete proofs for the lemmas and theorems presented in this section can be found in [13]. Indeed, a PDF in a given acyclic sequential circuit corresponds to a SDF in the TEM of the circuit. Similar to the case of combinational circuits with PDFs in the previous section, we first introduce two transformed circuits and their transformations that are used in the discussion on the test generation complexity of combinational circuits with SDFs.

Definition 8: A *segment-leaf-dag* C_S^{LD} for segment S ($S = \{g_1, g_2, \dots, g_m\}$) is a combinational circuit such that a fanout and an inverter are only permitted at g_1 of the segment S and the output of an inverter along S is not allowed to have a fanout.

The segment-leaf-transformation is defined analogously to the single-path-leaf transformation by considering segment S instead of path P [13].

Definition 9: The *S-edge* of segment S with starting point s in a segment-leaf-dag C_S^{LD} refers to the first connection of S after the inverter, if it exists. The S-edge is said to be associated with s .

Figure 3 shows a combinational circuit (a) and its segment leaf-dag for segment $s45e$ (b). We now define the segment transition-smoother STS that will be used to guarantee stable non-controlling values on the side inputs of OR gates (resp. AND gates) on segment S with rising SDF (resp. falling SDF).

Definition 10: A segment transition-smoother STS (Fig. 4) is a circuit with inputs V_0 and V_1 and outputs D_0 and D_1 . When $V_0 = V_1$, D_0 and D_1 have the same value as V_0 and

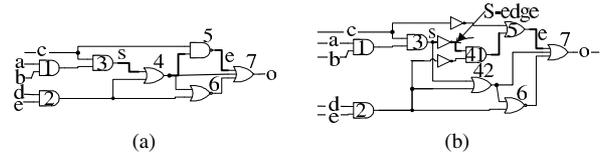


Fig. 3 (a) A combinational circuit (b) Its segment leaf-dag for segment $s45e$.

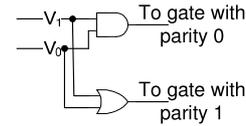


Fig. 4 Segment transition-smoother.

V_1 , respectively. When $V_0 \neq V_1$, D_0 becomes 0 while D_1 becomes 1.

Definition 11: A segment-leaf-dag C_S^{LD} for segment S can be transformed into a *segment-rising-smooth circuit* C_S^{RS} (resp. *segment-falling-smooth circuit* C_S^{FS}) for segment S by the *segment-rising-smooth* (resp. *segment falling-smooth*) transformation:

- S1& S2. Analogous to S1 and S2, respectively in Definition 5 by considering segment S instead of path P and the reverse topological traversal in S1 is performed on the transitive fanout of the primary inputs that are in the transitive fanin of g_1 on S ($= \{g_1, g_2, \dots, g_m\}$).
- S3. Let C_{2P} denote the transformed circuit after the above two steps. C_{2P} is called the second pattern partial circuit. Duplicate the transitive fanin of S-edge of C_{2P} as C_{1P} , which is called the first pattern partial circuit. Each primary input i_{1P} in C_{1P} has a corresponding primary input i_{2P} in C_{2P} . Each gate g_{1P} in C_{1P} has a corresponding g_{2P} in C_{2P} . Insert a segment transition-smoother STS to a primary input i_{2P} has an immediate gate with parity 0 or 1 by connecting the inputs i_{1P} of C_{1P} and i_{2P} of C_{2P} to the inputs V_0 and V_1 of STS, respectively and connecting D_0 and D_1 of STS to the immediate gates with parity 0 and 1, respectively. Note that when the segment S is also a path P , no first partial circuit C_{1P} is generated and this step is same as S3 in Definition 5.

The size of the resulting circuit is at most $6n - 5$ where n is the size of the circuit before transformation [13].

Figure 5 shows a combinational circuit with a SDF 345 \uparrow (a), its corresponding segment-leaf-dag for segment 345 (b) and its corresponding segment-rising-smooth circuit for 345 (c). The two-pattern test at the inputs ABC of the original circuit is $\langle 111, 101 \rangle$.

Lemma 8: Let n denote the size of a given combinational circuit C . The time complexity of the segment-leaf transformation on C is $O(n^2)$.

Lemma 9: Let C denote a segment-leaf-dag and $S \uparrow$ denote a rising SDF in C . The time complexity of the segment rising-smooth transformation on C is $O(n^2)$.

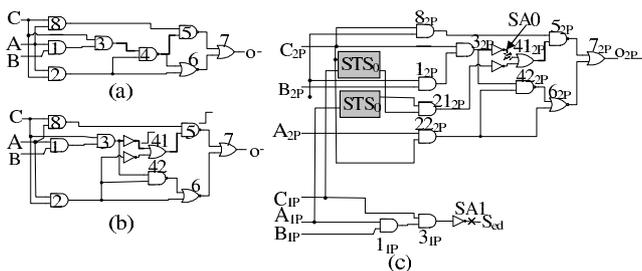


Fig. 5 (a) A combinational circuit. (b) Its segment leaf-dag for segment 345. (c) Its segment rising-smooth circuit for segment 345.

In the following subsection, we will show that the test generation problem for combinational circuits with SDFs is reducible to the test generation problem for its transformed circuits with double SAFs. The objective of the test generation problem for the segment-rising-smooth circuits with a double SAF is to generate tests that detect both faults simultaneously for a given pair of faults.

Lemma 10: The test generation complexity for segment-rising-smooth circuits C_S^{RS} with double SAFs is equivalent to the test generation complexity for combinational circuits with single SAFs, i.e. it is τ -equivalent.

Sketch of proof: The fault in the first pattern partial circuit of the segment smooth rising circuit is always at the line of the only primary output, the fault is tested if it is excited or assigned with a value that is opposite to the faulty value. In the case where the fault in the first pattern partial circuit is SA1 (resp. SA0), a new 2-input OR gate (resp. AND gate) is introduced to each primary output of the second pattern partial circuit where one input is connected to the primary output while the other input is connected to the only output of the first pattern partial circuit. The number of the new gates is at most the number of primary outputs of the second pattern partial circuit. The SA1 (resp. SA0) fault in the first pattern partial circuit is removed while the SA0 (resp. SA1) fault in the second pattern partial circuit remains. Let's called the modified circuit as modified segment smooth rising circuit. If a test pattern can detect the SA0 (resp. SA1) fault in the modified segment smooth rising circuit at a new primary output, then the test pattern can also excite the SA1 (resp. SA0) fault at the only primary output of the first pattern partial circuit in the segment smooth rising circuit and simultaneously detect the SA0 (resp. SA1) fault in the second pattern partial circuit of the segment smooth rising circuit. Therefore, the double SAF test generation of segment smooth rising circuits has same complexity as the single SAF test generation of combinational circuits. *q.e.d.*

Lemma 11: $\langle v_1, v_2 \rangle$ is a robust test for $S \uparrow$ in C_S^{LD} if and only if $u_2 = v_2 \sim v_1$ is a test for the double SAFs consisting of SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in C_S^{RS} where $v_2 \sim v_1$ denotes the concatenation of vectors v_2 and v_1 .

Sketch of proof: The test generation for the segment leaf-dag C_S^{LD} for S is reducible to the test generation for the cor-

responding segment rising-smooth circuit C_S^{RS} for S . The latter problem is further reducible to the test generation problem for C_S^{RS} with a double SAF of SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} . *q.e.d.*

Theorem 3: The test generation complexity for combinational circuits with robust SDFs is equivalent to the test generation complexity for combinational circuits with SAFs, i.e. it is τ -equivalent.

Sketch of proof: Lemma 11 shows the equivalence of the test generation for combinational circuits with SDFs and its segment rising-smooth circuits with SAFs at the S-edges, which is τ -bounded. Lemmas 8-10 prove that the former problem is reducible to the latter in time $O(n^2)$. A segment-rising-smooth circuit is also a path rising-smooth circuit when the starting point and the ending point of a segment S are also the primary input and the primary output of the circuit, respectively. Therefore path rising-smooth circuits is a subclass of segment-rising-smooth circuits. Assume the test generation for combinational circuits with robust SDFs is not τ -equivalent, then by using transformation δ , the test generation for combinational circuits with SAFs is not τ -equivalent from Lemmas 4 and 5 either, which is a contradiction. *q.e.d.*

Similarly, we can analyze the test generation complexity for non-robust SDFs by looking merely at the segment leaf-dag and the related transformations.

Theorem 4: The test generation complexity for combinational circuits with non-robust SDFs is equivalent to the test generation complexity for combinational circuits with SAFs, i.e. it is τ -equivalent.

5. Acyclic Sequential Circuits with Path Delay Faults

Based on the theoretical results in the previous section, we address the reducibility of the test generation for acyclic sequential circuits with PDFs to that for combinational circuits with SAFs. When generating tests for PDFs, we consider only slow-fast-slow clocking scheme. In slow-fast-slow clock scheme, justification phase and propagation phase are done at slow clock such that the circuit can be considered fault-free during these phases while the phase of deriving tests to excite the fault is done at normal operational clock or rated clock.

Lemma 12: Let $\langle v_1, v_2 \rangle$ denote a two-pattern test of a given balanced sequential circuit with size n . The time complexity of the sequence transformation to obtain $\langle v_1, v_2 \rangle$ from the test pattern generated for the combinational equivalent is $O(n)$.

Theorem 5: [10] The test generation problem for a balanced sequential circuit S^B with PDFs can be reduced to the test generation problem for its combinational equivalent $C(S^B)$ with SDFs.

Theorem 6: The test generation complexity for balanced sequential circuits with PDFs under rated clock and slow-fast-slow clock is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ -equivalent.

Proof: According to Theorem 5, the test generation for balanced sequential circuits with PDFs is equivalent to the test generation for its combinational equivalents with SDFs. In the previous section, we showed that the test generation for combinational circuits with SDFs is τ -equivalent. Based on Theorem 5, the theorems and lemmas of the test generation for combinational circuits with SDFs, the theorem is proved. *q.e.d.*

Lemma 13: Let x and y denote two different primary inputs of TEM $C_E(\mathcal{S}^A)$ of an acyclic sequential circuit \mathcal{S}^A . To avoid conflicts during sequence transformation Γ to obtain the two-pattern test from the test pattern generated on $C_E(\mathcal{S}^A)$ [12], $v_x^2 = v_y^1$ if x and y are corresponding to the same primary input z in \mathcal{S}^A and signals on y are the signals to be assigned to z one clock cycle later than are signals on x , where v_x^2 (resp. v_y^1) is the second pattern (resp. the first pattern) at x (resp. y) in the TEM.

Definition 12: Let x and y denote two different primary inputs of $C_E(\mathcal{S}^A)$. x and y are called **pattern-dependency input pair** (x, y) if x and y are corresponding to the same primary input z in \mathcal{S}^A and signals on y are the signals to be assigned to z one clock cycle later than are signals on x .

Definition 13: Given a segment leaf dag $C_S^{LD}((\mathcal{S}^A))$ of a TEM $C_E(\mathcal{S}^A)$ of \mathcal{S}^A , the circuit can be transformed into a **pattern-dependency circuit** $C_S^{PD}(\mathcal{S}^A)$ by the **pattern-dependency transformation**.

- S1. In the case of non-robust test generation, duplicate the transitive fanin of S-edge of C_S^{LD} where the segment leaf dag C_S^{LD} becomes the second pattern partial circuit C_{2P} while the duplicate becomes the first pattern partial circuit C_{1P} . In the case of robust test generation, perform the segment-rising-smooth (resp. segment-falling-smooth) transformation on C_S^{LD} .
- S2. For each pattern-dependency input pair (x, y) of $C_E(\mathcal{S}^A)$, connect the corresponding x_{2P} and y_{1P} to form a new primary input called unified input w . The resulting circuit is called pattern-dependency circuit $C_S^{PD}(\mathcal{S}^A)$, where x_{2P} (resp. y_{1P}) is the input in C_{2P} (resp. C_{1P}) corresponding to x (resp. y) in $C_E(\mathcal{S}^A)$.

The idea of pattern-dependency was introduced in [12]. Figure 6 shows the transformations of an acyclic sequential circuit into its pattern-dependency circuit to represent its test generation problem for PDFs based on the test generation for SAFs. Note that only one PDF is considered, that is in block 21, under slow-fast-slow clock. When registers $a - e$ in the acyclic sequential circuit in Fig. 6 (a) are transformed into its TEM in Fig. 6 (b), all registers are changed to wires and some blocks are duplicated. For example, blocks 21 and 22 correspond to block 2 in Fig. 6 (a). When the TEM is

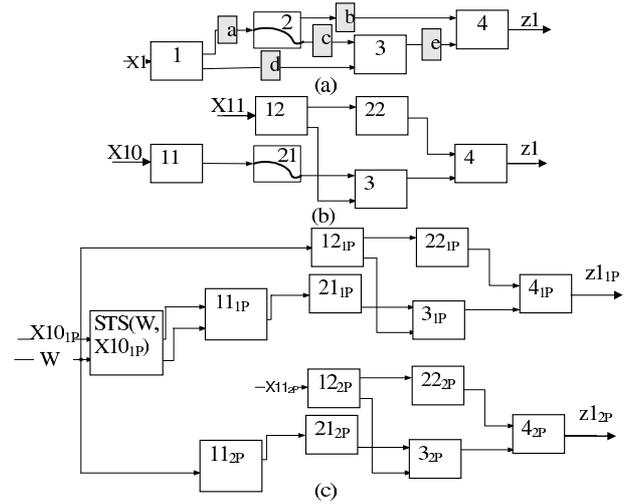


Fig. 6 (a) An acyclic sequential circuit. (b) Its TEM. (c) Its pattern-dependency circuit.

transformed into its pattern-dependency circuit in Fig. 6 (c), some blocks are also duplicated. For example, block 21_{1P} in the first pattern partial circuit and block 21_{2P} in the second pattern partial circuit correspond to block 21 in the TEM.

Definition 14: Given a pattern-dependency circuit $C_S^{PD}(\mathcal{S}^A)$ derived from a given acyclic sequential circuit \mathcal{S}^A , let C_{1P} and C_{2P} denote the first pattern partial circuit and the second pattern partial circuit of $C_S^{PD}(\mathcal{S}^A)$, respectively. Let $v_1^1, v_2^1, \dots, v_m^1$ of an m -bit vector v_1 denote a vector bit at each primary input of C_{1P} of $C_S^{PD}(\mathcal{S}^A)$ or the stem of the primary input fanout branches fed to C_{1P} of $C_S^{PD}(\mathcal{S}^A)$ if the input is a unified input, respectively where m is the number of vector bits. Let $v_1^2, v_2^2, \dots, v_m^2$ of an m -bit vector v_2 denote a vector bit at each primary input of C_{2P} of $C_S^{PD}(\mathcal{S}^A)$ or the stem of the primary input fanout branches fed to C_{2P} of $C_S^{PD}(\mathcal{S}^A)$ if the input is a unified input, respectively where m is the number of vector bits. $d(v_1, v_2)$ denote the input vector of the pattern-dependency circuit $C_S^{PD}(\mathcal{S}^A)$.

Lemma 14: Let P be a path in a given acyclic sequential circuit \mathcal{S}^A and let S_{2P} and S_{1P} be the corresponding segments in its pattern-dependency circuit $C_S^{PD}(\mathcal{S}^A)$. Let $d(v_1, v_2)$ be an input pattern for $C_S^{PD}(\mathcal{S}^A)$. Let $\Gamma_L(v_1, v_2)$ denote a two-pattern sequence of length L transformed from the two-pattern vector $\langle v_1, v_2 \rangle$ by the sequence transformation Γ . $\Gamma_L(v_1, v_2)$ is a robust (resp. non-robust) two-pattern sequence for the $P \uparrow$ in \mathcal{S}^A with sequential depth $L - 2$ if and only if $d(v_1, v_2)$ is a test for SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^A)$ with (resp. without) STS.

In Lemma 14, only rising SDFs are discussed. The lemma for falling SDF can be derived by considering SA1 at the S-edge of S_{2P} and SA0 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^A)$.

Theorem 7: The test generation complexity for internally balanced sequential circuits with PDFs under rated clock and slow-fast-slow clock is equivalent to the test generation

complexity for combinational circuits with SAFs, i.e. it is τ -equivalent.

Proof: Lemma 14 shows that the test generation for internally balanced sequential circuits with PDFs is equivalent to the test generation for pattern dependency circuits with SAFs at S-edges while Lemmas 8-10 prove that the former is reducible to the latter in $O(n^2)$. To show that the test generation for internally balanced sequential circuits with PDFs is τ -equivalent, we also have to prove that the test generation for combinational circuits with SAFs is equivalent to that for a subclass of internally balanced sequential circuits with SAFs. Since test generation for balanced sequential circuits with PDFs is τ -equivalent, the test generation for internally balanced sequential circuits with PDFs is equivalent to the test generation for combinational circuits with SAFs, which is τ -equivalent. *q.e.d.*

Theorem 8: The test generation complexity for acyclic sequential circuits with PDFs under slow-fast-slow clock is τ^2 -bounded.

Proof: Let T_{SL} , T_{PD} , T_C^{mSA} and T_P denote the time complexity of the segment-leaf transformation, the pattern-dependency circuit transformation, the test generation for double SAFs and the two-pattern sequence transformation, respectively. Let N_{SL} , N_{PD} , N_C^{mSA} and N_P denote the problem size of the segment-leaf transformation, the pattern-dependency circuit transformation, the test generation for double SAFs and the two-pattern sequence transformation, respectively. Let \mathcal{S}^A denote a given acyclic sequential circuit. The size of its TEM $C_E(\mathcal{S}^A)$ is $(d+1)n$ where d is the sequential depth. For $n \leq N_{SL} \leq (d+1)n$, $n \leq N_{PD} \leq 2((d+1)n)$, $2n \leq N_C^{mSA} \leq 6((d+1)n) - 5$, $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_A^{PD}(n) &= T_{SL}(N_{SL}) + T_{PD}(N_{PD}) \\ &\quad + T_C^{mSA}(N_C^{mSA}) + T_P(N_P) \\ &= O(\tau^2(n)) \text{ since } d = O(n) \end{aligned}$$

q.e.d.

Besides the test generation for PDFs under slow-fast-slow clock, there are analogous issue for the case under rated clock testing.

Open Problem 1: Is the test generation complexity for acyclic sequential circuits with PDFs under rated clock τ^2 -bounded?

Theorem 9: The test generation complexity for acyclic sequential circuits with PDFs under TEM at slow-fast-slow clock is not τ -equivalent.

There might exist also other test generation models for acyclic sequential circuits with PDFs besides TEM. Consequently, we have the following conjecture.

Conjecture 1: The test generation complexity for acyclic sequential circuits with PDFs under slow-fast-slow clock is not τ -equivalent.

Also, we have not yet considered the case under rated clock. Open Problem 2 corresponds to Theorem 9 and Conjecture 1.

Open Problem 2: Is the test generation complexity for acyclic sequential circuits (under TEM or other test generation models) with PDFs under rated clock τ -equivalent?

Answering these open problems would be useful in development of ATPG and DFT.

6. Cyclic Sequential Circuits with Stuck-At and Path Delay Faults

Generally, the test generation for cyclic sequential circuits with SAFs (resp. PDFs) involves derivation of the excitation state for the SAF (resp. PDF), state justification and state differentiation. In this section, we introduce an easily testable class of sequential circuits, namely two-column distributive SSFSM realizations (2CD-SSFSM). We address the test generation complexity for this class with SAFs and PDFs, and the relationship between the test generation problems. We assume a slow-fast-slow clock is used during testing. From this assumption, we derive that their test generation for PDFs may be easier or equivalent to the test generation for SAFs.

Formally, a finite state machine FSM is defined as a 5-tuple (I, ST, O, DEL, GAM) where I is a set of input symbols, ST is a set of states, O is a set of output symbols, $DEL : I \times ST \rightarrow ST$ is the next-state function, and GAM is the output function [15].

A state-shiftable finite state machine [14] with p states is a machine that possesses

1. transfer sequences of length at most $\lceil \log_2 p \rceil$ to carry the machine from state s_0 to state s_i for all i , and
2. distinguishing sequences of length $\lceil \log_2 p \rceil$, which are arbitrary input sequences consisting of two input symbols.

The degree of a state-shiftable finite state machine is equal to $\lceil \log_2 p \rceil$. Figure 7 (a) shows the state diagram of a state-shiftable finite state machine of degree 2 and Fig. 7 (b) illustrates its state diagram. IS denotes input symbol while PS denotes present state.

Definition 15: *Distributive SSFSM* is a two-column SSFSM with different pairs of input symbols for each state. Let the input symbols of two-column for state s_j be denoted by $\gamma_0(s_j)$ and $\gamma_1(s_j)$, respectively. Let ϵ_0 and ϵ_1 denote the input symbols of a two-column SSFSM, which has same degree with the distributive SSFSM. For each j , the next state function δ is such that $\delta(\epsilon_0, s_j) = \delta(\gamma_0(s_j), s_j)$ and $\delta(\epsilon_1, s_j) = \delta(\gamma_1(s_j), s_j)$.

Figure 7 (c) and Fig. 7 (d) shows the state diagrams and state tables for a distributive SSFSM.

Definition 16: Two-column distributive SSFSM realization

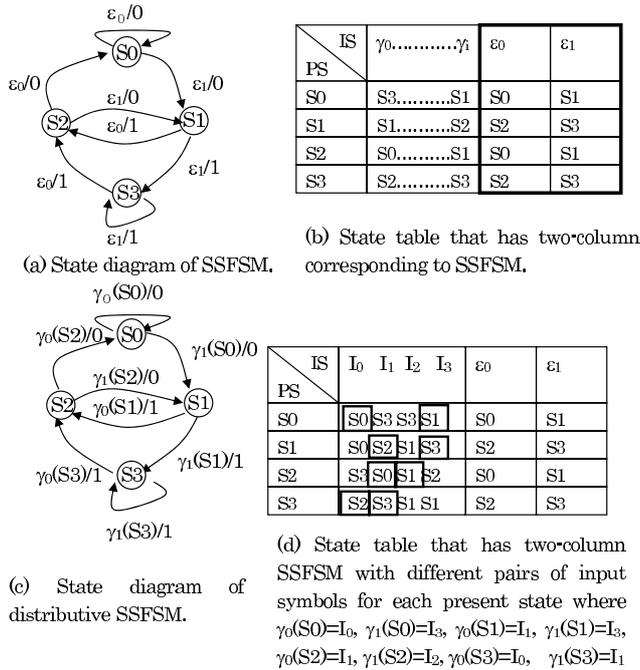


Fig. 7 State diagrams and state tables for SSFSM and distributive SSFSM.

tion (2CD-SSFSM) is an SSFSM realization that fulfills the following conditions:

- C1. There exists a two-column submachine of SSFSM of degree m in its state table, where $m = O(n)$ and n is the size of the 2CD-SSFSM. Let the input symbols of the two-column be denoted by ϵ_0 and ϵ_1 .
- C2. There exists a distributive submachine of SSFSM over the columns other than those of ϵ_0 and ϵ_1 . The number of columns is $2^{N-1} + 2$ where N is an integer.
- C3. There exists an input symbol c and a state s_j for $0 \leq j \leq m-1$ such that $s_k = \delta(c, s_j)$ and $s_k \neq \delta(\epsilon_0, s_j)$, $s_k \neq \delta(\epsilon_1, s_j)$ for $k \neq j$ and $0 \leq k \leq m-1$.
- C4. Let C_0 and C_1 denote the input combinations of ϵ_0 and ϵ_1 respectively after the input assignment. C_0 and C_1 are two-bit assignments, such that $C_0 = ab'$ and $C_1 = ab$ where a, b are variables for primary inputs and a is complement in other input combinations.

$$SHIFT = C_0 + C_1$$

$$D_0 = C_0 \text{ OR } F_0$$

⋮

$$D_i = (C_0 + C_1) \text{ AND } Q_{i-1} \text{ OR } F_i$$

⋮

$$D_{m-1} = (C_0 + C_1) \text{ AND } Q_{m-2} \text{ OR } F_{m-1}$$

$$O_{ss} = (C_0 + C_1) \text{ AND } Q_{m-1} \text{ OR } F_{O_{ss}}$$

Q_i (resp. D_i) is an output (resp. input) of flip-flop bit i . Gate sharing is permitted during the synthesis. A OR B (resp. A AND B) means both implicants are ORed (resp. ANDed) together. F_0, F_i, F_{m-1} and $F_{O_{ss}}$ are 0 and independent of states under the input cubes contained by both \bar{C}_0 and \bar{C}_1 .

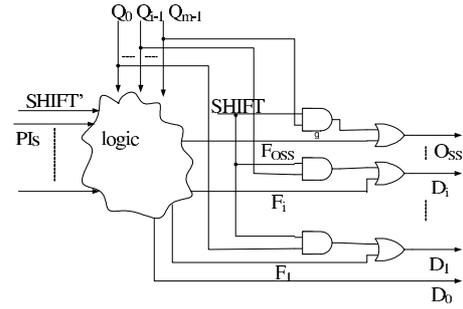


Fig. 8 General block diagram of a two-column distributive SSFSM realization.

Figure 8 shows the general block diagram of a 2CD-SSFSM. The following discusses the test generation complexity for SAFs and PDFs.

6.1 Test Generation Complexity for Stuck-At Faults

Theorem 10: The test generation complexity for 2CD-SSFSM with SAFs is τ^2 -bounded.

Sketch of proof: The realization of logic $C_0 + C_1$ is eventually an input, namely SHIFT that is ANDed with Q_{i-1} for $i > 0$ (Fig. 8). The justification sequence is an input sequence consisting of ϵ_0 and ϵ_1 with length at most $m-1$. Shifting operation fails when a s-a-0 occurs at SHIFT or at the output of SHIFT AND Q_{i-1} . The latter can always be activated and differentiated in shifting operation since the fault location is in the fanout-free region and the shifting operation of all the more significant flip-flops are still working. Looking in the former case where the fault is at the stem of SHIFT, the shifting operation of the circuit fails. However, the distributive shifting operation is intact. For other faults, shifting operation always works. First, the SAF activation is performed at $\tau(n)$. To differentiate a pair of fault-free and faulty states after SAF activation, the fault effect at a flip-flop is propagated to the output O_{ss} by searching the input sequence on its iterative logic array of size at most $m-1$. Since $m = O(n)$, the time complexity of the differentiation is $O(\tau^2(n))$. Let T_E, T_J and T_D denote the time complexity of SAF excitation, justification and differentiation. The test generation for other faults is easier. Therefore,

$$\begin{aligned} T_{2CD}^{SA}(n) &= T_E(n) + T_J + T_D \\ &= \tau(n) + O(m-1) + O(\tau((m-1)n)) \\ &= O(\tau^2(n)) \text{ for } m = O(n) \end{aligned}$$

q.e.d.

However, we cannot conclude that the test generation complexity for 2CD-SSFSM with SAFs is not τ -equivalent although it seems to be correct.

Conjecture 2: The test generation complexity for 2CD-SSFSM with SAFs is not τ -equivalent.

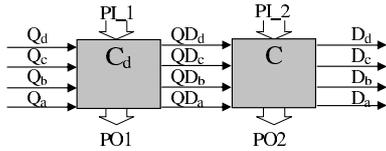


Fig. 9 A duplex combinational circuit.

6.2 Test Generation Complexity for Path Delay Faults

Definition 17: Let P and P' denote a path in a given cyclic sequential circuit S^C and the corresponding path in its combinational part c . A **duplex combinational circuit** $C_P^D(S^C)$ for P (Fig. 9) of a cyclic sequential circuit S can be obtained by the following transformation:

- S1. Perform the single-path-leaf transformation for P' on c . The inputs of c corresponding to the outputs of the flip-flops in S^C are called the pseudo inputs while the outputs of c corresponding to the inputs of the flip-flops in S^C are called the pseudo outputs. The resulting single-path leaf-dag is denoted by $c_{P'}^{LD}$.
- S2. Duplicate $c_{P'}^{LD}$. The single-path leaf-dag $c_{P'}^{LD}$ and its duplicate are named as the first partial circuit c_1 and the second partial circuit c_2 .
- S3. Connect the pseudo outputs of c_1 to the corresponding pseudo inputs of c_2 to form an iterative logic array of single-path leaf-dag of size 2. The new connections between c_1 and c_2 are called pseudo interconnections and a pseudo interconnection is labeled as QD_i while a resulting pseudo input and pseudo output are labeled as Q_i and D_i respectively, corresponding to flip-flop i in S^C . Note that the path P in S^C corresponds to two segments S_{c1} and S_{c2} in $C_P^D(S^C)$. A primary input and a primary output of c_1 is denoted by I_{1j} and O_{1k} , respectively while a primary input and a primary output of c_2 is denoted by I_{2j} and O_{2k} .

Definition 18: Let $P \uparrow$ denote a rising PDF in a given cyclic sequential circuit S^C . A duplex combinational circuit $C_P^D(S^C)$ for P can be transformed into a **path-rising-smooth duplex circuit** (resp. **path-falling-smooth duplex circuit**) $C_S^{PRS}(S^C)$ (resp. $C_S^{PFS}(S^C)$) for the corresponding segment S_{c2} by the following procedure:

- S1. Let Q_{OR} (resp. Q_{AND}) denote the OR gates (resp. AND gates) along S_{c2} corresponding to $P \uparrow$ (resp. $P \downarrow$). A gate may have no parity, 0, 1 or both parities. A side-input to an OR gate (resp. AND gate) in Q_{OR} (resp. Q_{AND}) has parity 1 (resp. 0). Perform a reverse topological traversal from the transitive fanout of all pseudo interconnections, to determine the parity of all gates along the side-paths to S_{c2} . The parity is complemented across a NOT gate. If some fanouts of a gate have parity 1 and others have parity 0, the gate is assigned both parities.
- S2. Duplicate gates so that each resulting gate has parity of

either nothing, 0 or 1 but not both.

- S2.1. Traversing from pseudo output or primary output g_m on P , for each gate h_j with a parity (parities) and with a successor gate that is off path and without parity, h_j and the connections of its immediate predecessor gates are duplicated once and its duplicate h'_j has no parity. For each immediate successor gate h_{j+1} of h_j that has no parity, the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1} .
- S2.2. Traversing from pseudo output or primary output g_m , each gate h_j with both parities and the connections to its immediate predecessor gates are duplicated once and assigned parity 1 while its duplicate h'_j is assigned parity 0. For each immediate successor gate h_{j+1} of h_j that has parity 0 (1 if there is an inversion between h_j and h_{j+1}), the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1} .
- S3. Insert to the fanout branch of a second circuit primary input I_{2j} a segment-transition-smoother $STS(I_{2j}, I_{1j})$ if the fanout branch has an immediate gate with parity 0 or 1. At the fanout branch of a pseudo interconnection QD_i , insert a segment transition-smoother $STS(QD_i, Q_i)$ if the QD_i has an immediate gate with parity 0 or 1.

Lemma 15: $\langle v_1, v_2 \rangle$ is an input sequence that robustly excites a PDF $P \uparrow$ (resp. $P \downarrow$) of a sequential circuit S^C in present state s_1 if and only if $s_1 \sim v_1 \sim v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint of 0 at the S-edge of S_{c1} in the corresponding path-rising-smooth duplex circuit $C_S^{PRS}(S^C)$.

Lemma 16: $\langle v_1, v_2 \rangle$ is an input sequence that non-robustly excites a PDF $P \uparrow$ (resp. $P \downarrow$) of a sequential circuit S^C in present state s_1 if and only if $s_1 \sim v_1 \sim v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint of 0 at the S-edge of S_{c1} in the corresponding duplex combinational circuit $C_S^{PRS}(S^C)$.

Definition 19: A combinational circuit C with a SAF f can be transformed into a cyclic sequential circuit $S_f^{c\delta}$ (Fig. 10) by **cyclic δ transformation**:

- S1. Same as S1 in Definition 7.
- S2. Connect the output of $G(C, C_f)$ to a two-input AND gate. The output O of the AND gate A is fed back to the AND gate through an inverter I .

Lemma 17: v is a test for SAF f in a combinational circuit C if and only if $\langle v, v \rangle$ excites the PDF $IAO \uparrow$ or $IAO \downarrow$ in the corresponding cyclic sequential circuit $S_f^{c\delta}$.

Theorem 11: The derivation of PDF excitation state is τ -equivalent.

Proof: Lemmas 15 and 16 show that the derivation of PDF

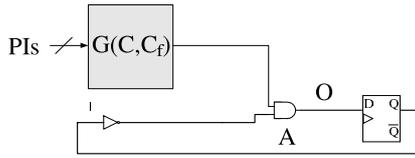


Fig. 10 A cyclic sequential circuit $S_f^{c\delta}$.

excitation state is equivalent to the test generation for path-rising-smooth duplex circuits and duplex combinational circuits with SAFs at S-edges, which is τ -bounded. The time complexity for the transformation between the two problems is $O(n^2)$ as described in Definitions 17 and 18. Assume the derivation of PDF excitation state is not τ -equivalent, then by using cyclic δ transformation, the test generation for combinational circuits with SAFs is not τ -equivalent from Lemma 17 either, which is a contradiction. *q.e.d.*

Theorem 12: The test generation complexity for two-column distributive SSFSM realization with PDFs under slow-fast-slow clock is equivalent to the test generation complexity for combinational circuits with SAFs, i.e. it is τ -equivalent.

We also have not yet solved the PDF test generation complexity of the 2CD-SSFSM under rated clock.

Open Problem 3: Is the test generation complexity for 2CD-SSFSM with PDFs under rated clock equivalent to the test generation complexity for combinational circuits with SAFs, i.e. it is τ -equivalent?

The test generation for 2CD-SSFSM with PDFs under slow-fast-slow clock is τ -equivalent while that with SAFs is τ^2 -bounded. In other words, if Conjecture 1 is proved, then 2CD-SSFSM would be a class whose test generation complexity for PDFs under slow-fast-slow clock is less than that for SAFs.

7. Conclusion

The time complexity and the relationships between the test generation problem for several existing classes of circuits with SAFs and PDFs have been described in this paper. The test generation for internally balanced sequential circuits with SAFs and PDFs under rated clock and slow-fast-slow clock is equivalent to the test generation for combinational circuits with SAFs. On the other hand, the test generation for the acyclic sequential circuits with SAFs and PDFs under slow-fast-slow clock is τ^2 -bounded. It is shown that under TEM at slow-fast-slow clock the test generation for PDFs is not τ -equivalent. For 2CD-SSFSM with PDFs under slow-fast-slow clock, its test generation complexity is τ -equivalent but that with SAFs is τ^2 -bounded. The test generation for 2CD-SSFSM with SAFs seems not to be τ -equivalent and remains as a conjecture. If it is proved, 2CD-SSFSM will be a class of circuits that has the test generation complexity for PDFs less than the test generation complexity for SAFs. The test generation for acyclic sequential cir-

cuits and cyclic sequential circuits with PDFs is discussed under the assumption of slow-fast-slow clock. Similar discussion is also needed for the condition under rated clock.

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