

PAPER

Effective Domain Partitioning for Multi-Clock Domain IP Core Wrapper Design under Power Constraints

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SUMMARY The rapid advancement of VLSI technology has made it possible for chip designers and manufacturers to embed the components of a whole system onto a single chip, called System-on-Chip or SoC. SoCs make use of pre-designed modules, called IP-cores, which provide faster design time and quicker time-to-market. Furthermore, SoCs that operate at multiple clock domains and very low power requirements are being utilized in the latest communications, networking and signal processing devices. As a result, the testing of SoCs and multi-clock domain embedded cores under power constraints has been rapidly gaining importance. In this research, a novel method for designing power-aware test wrappers for embedded cores with multiple clock domains is presented. By effectively partitioning the various clock domains, we are able to increase the solution space of possible test schedules for the core. Since previous methods were limited to concurrently testing all the clock domains, we effectively remove this limitation by making use of bandwidth conversion, multiple shift frequencies and properly gating the clock signals to control the shift activity of various core logic elements. The combination of the above techniques gains us greater flexibility when determining an optimal test schedule under very tight power constraints. Furthermore, since it is computationally intensive to search the entire expanded solution space for the possible test schedules, we propose a heuristic 3-D bin packing algorithm to determine the optimal wrapper architecture and test schedule while minimizing the test time under power and bandwidth constraints.

key words: multi-clock domain, wrapper design, SoC, embedded core test, test scheduling

1. Introduction

The recent popularity of advanced technologies such as broadband internet, 3-G cellular phones and high-speed workstations is due to many factors, one of which is the rapid advancement in the design and production of VLSI chips. More importantly, it has now become possible to put entire systems onto a single chip which is commonly known as System-on-Chip (SoC). Currently, SoCs are widely used in devices intended for telecommunications, networking and digital signal processing. Moreover, they are increasingly being utilized in mobile on-the-field devices, which increase the demand for highly-reliable, defect-free chips that have very low power requirements.

To ensure that SoCs and other VLSI chips operate as intended, testing must be conducted per chip. As production capabilities improve, clock-rates rise exponentially and

transistor density increases dramatically, the cost of testing newer VLSI chips also becomes higher. More specifically, the increased complexity of the circuitry in SoCs also means an increase in the amount of test data, which usually results in longer test application time. Furthermore, test access becomes a problem since the cores cannot be directly accessed from the I/O pins of the chip. Moreover, modern IP cores operate at various frequencies internally, which have advantages such as reduced power and silicon area. These *multi-clock domain cores* present clock skew and at-speed testing problems. Clock skew problems arise from unsynchronized clock sources such as two signals of the same frequency but different clock trees that arrive out-of-sync to their destinations thereby causing data corruption. Furthermore, power consumption and heat during test has become a big issue because of high switching activity during scan-shift operations as well as the possibility of more active components than expected during normal operation.

The most common Design-for-Testability (DFT) used for SoCs with multiple cores is the design of a test data delivery method, more commonly known as Test Access Mechanism (TAM), and the use of *wrappers*, which enables independent core testing. The wrapper isolates a core during test and provides an interface to apply and collect test data from it. More recently, the IEEE 1500 standard for embedded core test has been approved to provide guidelines for core wrapper design and interfacing to TAMs. Furthermore, several approaches to optimize wrapper designs for single frequency embedded core testing [1], [2] as well as wrapper and TAM co-optimization algorithms [3], [4], [11], [12] have already been suggested. Still, these approaches don't directly address the problem of testing multi-clock domain cores.

To address this problem, we propose an IEEE 1500 compliant power-aware multi-clock domain core wrapper that partitions the IP core into smaller sub-groups and utilizes gated-clocks to control the start times of scan-shift operations and enable a more flexible and efficient use of the external bandwidth under a power constraint compared to previous methods. A heuristic 3-D rectangular bin packing algorithm is also introduced, which forms the basis of the proposed wrapper design method.

2. Related Work

Most at-speed multi-clock domain core testing techniques

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that have been proposed are based on BIST [5]–[7] and utilizing techniques such as programmable capture windows [5] and directly controlling separate launch and capture clocks [6] to solve the clock-skew problems while still allowing at-speed testing. The first non-BIST based multi-clock domain core wrapper design for IP cores was proposed in [8], where the core was divided into its clock domains, calling them virtual cores. Single frequency wrapper design was performed on each virtual core to assign a virtual wrapper to each of them. Virtual test bus lines from each virtual core are connected to the external TAM via de-multiplexing and multiplexing interfaces to synchronize the flow of the test data. The method employs a single separate shift clock for all virtual cores, and it is multiplexed with the capture clock signals. In [9], the authors of [8] improved upon their design by allowing each virtual core to have a distinct shift frequency. In both [8] and [9] all virtual cores are concurrently active and the lowering of shift frequencies that lead to large increases in test time might result under a tight power constraint. In [10], the use of gated-clocks to control the start and end times of the shift activity of each virtual core has been proposed. The authors used a 3-D bin packing algorithm which grouped virtual cores into *shelves* wherein all cores belonging to the same shelf become active at the same time and each shelf becoming active sequentially. This gives more flexibility during scheduling but can result in significant idle time because available bandwidth and power cannot be immediately used until the scan operation of the current shelf group is done.

This paper proposes a wrapper design method which uses a novel 3-D bin packing algorithm as its basis. The design allows for two things which improve upon previous work: (i) each clock domain can be further partitioned into sub domains and (ii) a virtual core can be activated as soon as bandwidth and power are available.

The rest of the paper is organized as follows. The overview of the proposed wrapper architecture and its scan-control block is given in Sect. 3. Section 4 gives the problem formulation and Sect. 5 discusses the proposed 3-D bin packing algorithm. Section 6 discusses the experimental results and compares them with the results of previous work and Sect. 7 concludes this paper.

3. Multi-Clock Domain Core Wrapper (MDCW)

In this paper, it is assumed that the clock domains of the IP-core can be further divided into sub-domains. Furthermore, we assume that the following information is provided by the core designer:

P_{max} : Maximum allowed peak or average power dissipation (during scan)

N_C : Number of clock domains

N_{si} : Number of sub-domains for each clock domain D_i ($1 \leq i \leq N_C$)

For each sub-domain S_{ij} ($1 \leq j \leq N_{si}$) of clock domain D_i

- pi_{ij} : Number of primary input pins

- po_{ij} : Number of primary output pins
- bi_{ij} : Number of bidirectional I/O
- sc_{ij} : Number of internal scan chains and their lengths l_{ijk} ($1 \leq k \leq sc_{ij}$)
- p_{ij} : Power dissipation at ATE frequency f_{ATE}

We now extend the definition of the virtual core from [8]. A group of one or more sub-domains from D_i is a virtual core G_{ip} ($1 \leq p \leq N_{gi}$). N_{gi} is the total number of possible combinations of the sub-domains of D_i . Furthermore, to differentiate from the virtual core defined in [8]–[10], we would refer to virtual core in this paper as *P-vc*, short for *Partitioned virtual core*, and denotes the fact that it can represent one complete clock domain or just a part of it.

Wrapper Architecture The basic architecture of the proposed multi-clock domain core wrapper is shown in Fig. 1. The core is divided into smaller *P-vc*'s, each having its own virtual wrapper. These *P-vc*'s are connected to the external TAM via *virtual test bus* lines and a pair of *de-multiplexing* and *multiplexing interface circuits* (DMIC-MIC) that perform bandwidth matching and test data flow-control between the external TAM and the internal virtual test bus lines.

Scan Control Block The scan control circuitry for the proposed wrapper is shown in Fig. 2. It is assumed that there are m external clock sources available, either from the Automatic Test Equipment (ATE) or on-chip PLL circuits. Furthermore, an external signal, *TestStart*, is triggered when the wrapper enters test mode. Normally, the test application process is divided into two phases, scan and capture phase. For this work, test data is scanned into the scan chains of each *P-vc* during the scan phase at a frequency that can be different from their functional frequencies. These scan clock signals are generated by the *Clock Divider* in Fig. 2. We add a *gate and MUX control circuit* to control N_{tot} (total number of *P-vc*'s) gated clock signals during test as well as switch to the functional clocks during normal operation. In the timing diagram of Fig. 3, test data is scanned into $P\text{-vc}_1$ until time $t1$, when it becomes inactive and $P\text{-vc}_2$ starts the scan operation at a different frequency until time $t2$. At $t2$, the process begins the capture phase.

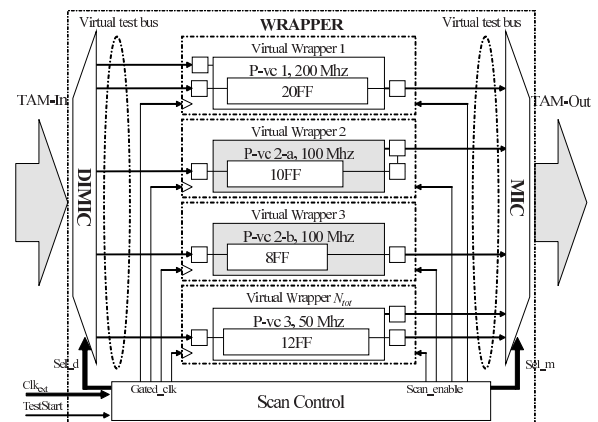


Fig. 1 Proposed multi-clock domain wrapper.

Grouping the wrapper scan chains according to their clock domains prevents the effects of clock skew during this phase. To avoid clock skew at the capture phase, the test enters this phase before or after the last bit of test data is scanned in. In the capture phase, all the scan chains are driven by their functional clocks to simulate normal operation. For multi-clock domain cores, a capture window similar to that proposed in [8],[9], as shown in Fig. 3, is used during this phase and the P -vc's are activated in such a way that ensures inter-domain and intra-domain signals are prop-

erly captured for analysis. A comparison of schedules obtained in [9], [10] and by our method is shown in Fig. 4. The use of gated clocks enables a more flexible and efficient test schedule compared to the concurrent shifting method in [9]. Unlike the shelf method in [10], our scheme allows partitioned testing with more flexibility and less wasted bandwidth during scheduling. Since we are using a capture window as proposed in [8],[9], this work will only focus on minimizing the shift time during the scan phase.

4. Problem Formulation

The wrapper design problem P_{MDCW} is defined as follows:

Problem P_{MDCW} : Given the test parameters for a multi-clock domain core C as described in Sect. 2 and the information below:

- W_{ext} : TAM width allotted to the core
- f_{ATE} : ATE frequency
- $F = \{f_1, f_2, \dots, f_m \mid f_j = 2 \times f_{j+1}, j \in 1, \dots, m - 1\}$: The set of allowed shift frequencies

determine the multi-clock domain wrapper design for C including:

N_{vi} : Number of P -vc's $G_{ip}(1 \leq p \leq N_{vi})$ under domain D_i
 For each P -vc G_{ip} of clock domain D_i

- $f_{ip} \in F$: Shift frequency
- w_{ip} : Number of virtual bus lines

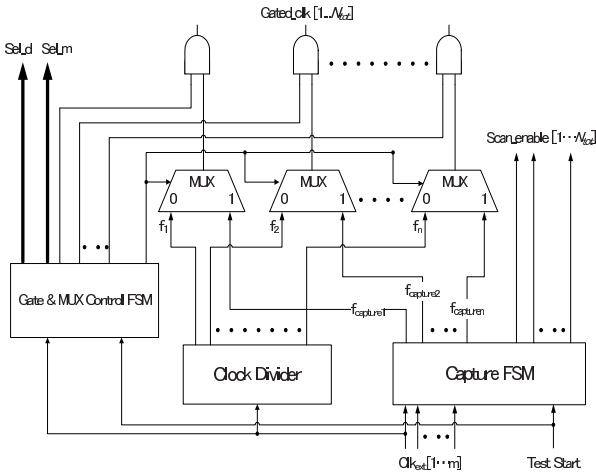


Fig. 2 Proposed scan control block.

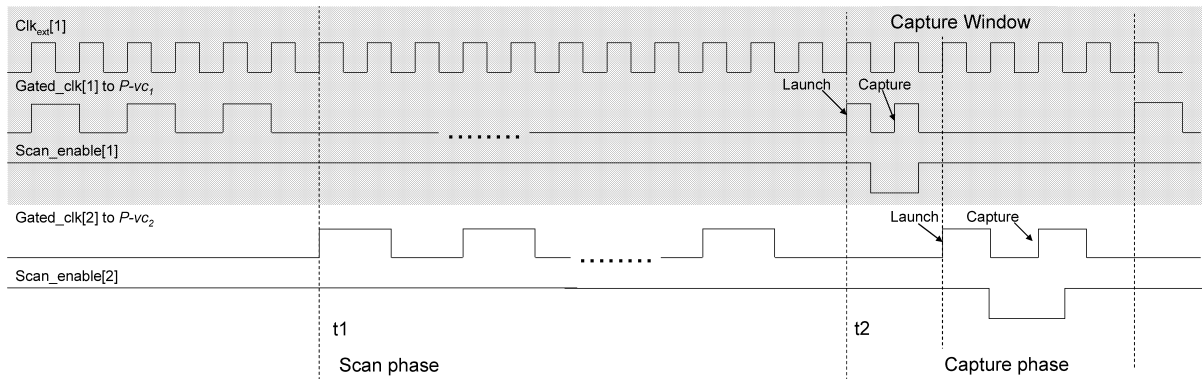


Fig. 3 Testing timing diagram.

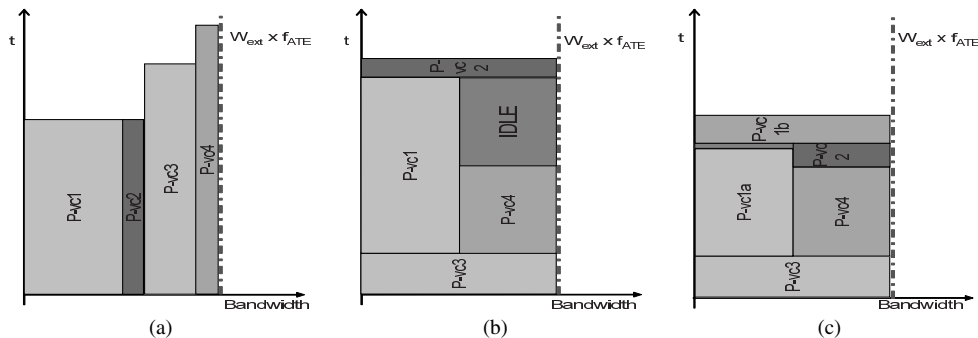


Fig. 4 Comparison of (a) concurrent scan in [9] (b) shelf method from [11] (c) using proposed method.

- Its wrapper scan chain design and l_{ipmax} , which is the length of its longest wrapper scan chain
- t_{sip} : Scan-in start time

such that the following constraints are satisfied and the test application time is minimized:

1. The bandwidth used by all the active P -vc's at any time t cannot exceed the total bandwidth coming from the ATE:

$$W_{ext} \times f_{ATE} \geq \max_{0 \leq t \leq T} \left(\sum_{i=1}^{N_c} \sum_{p=1}^{N_{ii}} a_{ipt} f_{ip} w_{ip} \right) \quad (1)$$

$$\text{where: } a_{ipt} = \begin{cases} 0, & t < t_{sip} \text{ or } t > (t_{sip} + l_{ipmax} \times \frac{f_{ATE}}{f_{ip}}) \\ 1, & t_{sip} \leq t \leq (t_{sip} + l_{ipmax} \times \frac{f_{ATE}}{f_{ip}}) \end{cases}$$

2. The total power dissipation of all active P -vc's at any time t cannot exceed the maximum allowed power dissipation P_{max} :

$$P_{max} \geq \max_{0 \leq t \leq T} \left(\sum_{i=1}^{N_c} \sum_{p=1}^{N_{ii}} a_{ipt} P_{ip} \times \frac{f_{ip}}{f_{ATE}} \right) \quad (2)$$

Since all the P -vc's become active and inactive independently, the total scan-shift time for one test pattern can be computed from the P -vc with the latest end time as shown below:

$$T = \max_{1 \leq i \leq N_c} \left(\max_{1 \leq p \leq N_{ii}} \left(t_{sip} + l_{ipmax} \times \frac{f_{ATE}}{f_{ip}} \right) \right) \quad (3)$$

Each P -vc will have a distinct shift frequency and to simplify the clock generation circuitry, the ratio of usable frequencies is a two's exponent. Our initial experiments have shown that completely dividing cores into sub-domains wouldn't always yield shorter test times so we developed a 3-D bin packing algorithm to determine how and when the domains should be partitioned to minimize the scan-shift time T while also optimizing the final number of P -vc's.

5. Proposed Test Scheduling Algorithm

Similar to [4], rectangular 2-D bin packing have been extensively used to solve the test scheduling problem for embedded cores. For scheduling under a power constraint, it can be extended into a restricted 3-D bin packing problem where the length, width and height represent pin, peak power and total test time, respectively, of an SoC [12]. Specifically, a core (or in our case, P -vc), is represented as a cube whose length, width and height represents the allotted TAM width, power dissipation and test time, and when a cube overlaps in the time domain, they cannot overlap at any of the other two domains. In this paper, instead of pin count or TAM width, the length represents the external bandwidth $BW_{ext} = W_{ext} \times f_{ATE}$ and each P -vc G_{ip} of an IP-core C can be represented by one cube among a set of permissible cubes. The cubes are packed into the 3-D bin until all the sub-domains S_{ij} of each domain D_i have been included in

Table 1 hCADT01 clock and sub-domain information.

sd#	f_{func} (MHz)	N_{in}	N_{out}	N_{bi}	P	N_{sc}	Lsc_{ij}
1.1	200	50	8	18	668	4	168, 168, 166, 166
1.2	200	25	8	18	652	4	163, 163, 163, 163
1.3	200	25	8	18	648	4	162, 162, 162, 162
1.4	200	9	8	18	604	4	151, 151, 151, 151
2.1	133	144	67	72	450	3	150, 150, 150
3.1	120	39	4	24	465	5	93, 93, 93, 93, 93
3.2	120	30	3	24	279	3	93, 93, 93
3.3	120	20	1	24	186	2	93, 93
4.1	75	61	10	36	657	3	219, 219, 219
4.2	75	50	21	36	657	3	219, 219, 219
5.1	50	87	200	36	1563	3	521, 521, 521
5.2	50	30	24	36	1042	2	521, 521
6.1	33	96	10	24	278	5	82, 81, 81, 17, 17
6.2	33	30	18	24	198	4	82, 81, 18, 17
6.3	33	20	40	24	100	2	82, 18
7.1	25	15	30	72	40	4	10, 10, 10, 10

the packed P -vc's while minimizing the total height. Since it has been shown that the restricted 3-D bin packing problem is NP -Hard in [12], we propose the following heuristic algorithm to solve the problem.

5.1 Initialization: Cube Creation and Ordering

To illustrate the various steps in the algorithm, the benchmark multi-clock domain IP core *hTCADT01*, first introduced in [9] and shown in Table 1, is used throughout the following sections. This IP core has seven clock domains and $sd\#$ denotes the sub-domain number while P is the power dissipation of the sub-domains when shifting at 100 MHz and is made equal to the sum of all the scan chain lengths Lsc_{ij} belonging to that sub-domain to simplify the setup. Further details are given in Sect. 6.

P -vc's can be created to represent any combination of sub-domains belonging to the same clock domain. If a domain D_i has N_{si} sub-domains, then the total number of possible P -vc's from D_i is just the sum of all the possible combinations of S_{ij} .

$$N_{gi} = \sum_{j=1}^{N_{si}} N_{sj} C_j \quad (4)$$

Single frequency wrapper design such as in [3] is performed on all P -vc's. In [3], given the allotted virtual test bus width, the I/O boundary scan cells and internal scan chains are connected into wrapper scan chains in such a way that length of the longest wrapper scan chain, l_{ipmax} , is minimized. l_{ipmax} determines the test time for the core (Eq. 7) and it can vary depending on the allotted test bus width. For example, the l_{ipmax} for domain 7 in Table 1 at $w_{ip} = 15$ and 3 is 10 and 48, respectively. At $f_{ip} = 100$ MHz, this will give us test times of $0.10 \mu\text{sec.}$ and $0.48 \mu\text{sec.}$, respectively. We denote the maximum number of virtual test bus lines that can be assigned to a P -vc as Vtb_{max} . Each P -vc G_{ip} ($1 \leq p \leq N_{gi}$) can have a maximum of Vtb_{max} possible wrapper designs and the same number of cubes is created.

From the list of cubes of G_{ip} , the cube with the shortest test time regardless of power or bandwidth constraints would be selected as its ideal cube. It was proven in [10] that halving the shift frequency of the P -vc while doubling the virtual test bus width can result in either an increase in scan-shift time or no increase at all. We take advantage of this property to maintain the test time while still minimizing the power dissipation of the core. Each P -vc G_{ip} is expressed as a triplet $C_{ip} = \{BW_{ip}, p_{ip}, t_{ip}\}$, where $BW_{ip} = w_{ip} \times f_{ip}$ is the bandwidth of G_{ip} , w_{ip} is the virtual test bus width assigned to it, and $f_{ip} \in F$ represents its shift frequency. The power dissipation p_{ip} at f_{ip} can be expressed as:

$$p_{ip} = \frac{p_{ipmax} \times f_{ip}}{f_1} \quad (5)$$

where f_1 is the maximum allowed shift frequency. In this paper, we set $f_1 = f_{ATE}$ and p_{ipmax} is the power dissipation at f_1 as expressed below:

$$p_{ipmax} = \sum_{j=1}^{N_{sj}} b_{ij} p_{ij} \quad (6)$$

where $b_{ij} = 1$ when sub-domain S_{ij} belongs to G_{ip} and $b_{ij} = 0$ if not, and p_{ij} is the power dissipation of S_{ij} at f_{ATE} . The minimum test time t_{ip} can be computed as follows:

$$t_{ip} = \frac{t_{ipmax}}{f_{ip}} \quad (7)$$

The ideal cubes of P -vc's representing whole domains that satisfy the bandwidth and power restrictions is put into a master cube list L_M . The remaining ideal cubes not in L_M but satisfy the bandwidth and power constraints are then added to it. Finally, the ideal cubes of P -vc's representing only one sub-domain is then added to L_M to ensure that all sub-domains are tested in the final schedule. Then, an area attribute $A_{ip} = BW_{ip} \times t_{ip}$ is also computed for each cube of P -vc's representing single sub-domains. Since the bigger the area attribute, the harder it is to pack, it follows that sub-domain groups which have big sub-domains must be prioritized by sorting L_M from the cube of the P -vc that has the member sub-domain with the biggest area attribute to the P -vc with the smallest one. If two cubes have the same sized sub-domains, then the overall area attribute of the cubes themselves are compared during sorting. After the list preparations, bin packing can be started from Step 1.

5.2 Step 1: Packing Domain Cubes

Before packing, the algorithm takes note of the current time in the schedule, denoted by a variable $curr_time$. Since the algorithm only divides domain P -vc's when necessary, in this step the algorithm only looks at cubes representing whole domains in L_M until it finds a cube that has $p_{ip} \leq p_{avail}$ and $BW_{ip} \leq BW_{avail}$. p_{avail} is the available power and BW_{avail} is the available bandwidth, respectively. If a cube is found and packed into the bin, the algorithm checks

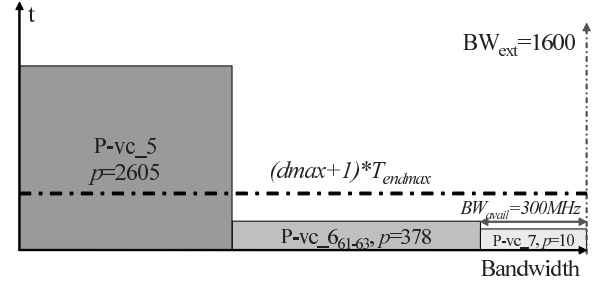


Fig. 5 Packing results from steps 1-3.

what sub-domains belong to it and updates L_M by removing all cubes that has at least one member sub-domain equal to any of the sub-domains of the packed P -vc. It continues the above process until (a) $BW_{avail} = 0$ and/or $p_{avail} = 0$ or (b) if a proper cube cannot be found. Under condition (a), the algorithm looks among currently scheduled P -vc's for the P -vc with the earliest test end time and sets $curr_time$ equal to it and repeats Step 1. Under condition (b), the algorithm proceeds to Step 2. For the benchmark core *hTCAD01* [9] shown in Table 1 with external bandwidth $BW_{ext} = 1600$ and $P_{max} = 3000$, Step 1 packs the P -vc of domain no.5 (P -vc that combines sub-domain 5.1 and 5.2 from Table 1) with power $p = 2605$, as shown in Fig. 5.

5.3 Step 2: Packing Sub-Domain Group Cubes

Not finding a cube in Step 1 means that partitioning a domain is necessary. In Step 2 the algorithm only looks at the cubes not tried in Step 1, which represent sub-domain groups, until it finds a cube that satisfies $p_{ip} \leq p_{avail}$ and $BW_{ip} \leq BW_{avail}$. If a cube is found and packed into the bin, the algorithm again checks what sub-domains belong to it and updates L_M . Step 2 is repeated while there is available power and bandwidth or if a proper cube cannot be found. If BW_{avail} and/or p_{avail} become zero, $curr_time$ is again updated and the algorithm goes back to Step 1. But if a proper cube cannot be found, the algorithm proceeds to Step 3. In Fig. 5, Step 2 is illustrated when the P -vc of sub-domain group $S_{61} \cup S_{63}$ of domain 6 is packed into the bin.

5.4 Step 3: Filling Idle Space by Decreasing Virtual Test Bus Lines

In Step 3, the algorithm searches for the packed cube using the biggest bandwidth and denotes its test end time as T_{endmax} . L_M is then traversed for a cube that satisfies p_{avail} . It then determines the new scan-shift time t_{ipnew} for the cube being tried given a new bandwidth $BW_{ipnew} = BW_{avail}$. Because of the limited selection of usable shift frequencies, choosing the next lowest f_k would automatically lead to a doubling of the scan-shift time. So for Step 3, the assigned virtual test bus width is decreased and t_{ipnew} is computed. The shift frequency is halved and the virtual test bus is doubled to minimize power as long as t_{ipnew} remains constant. If $t_{ipnew} \leq T_{endmax} \times (1 + dmax)$, then the cube is packed

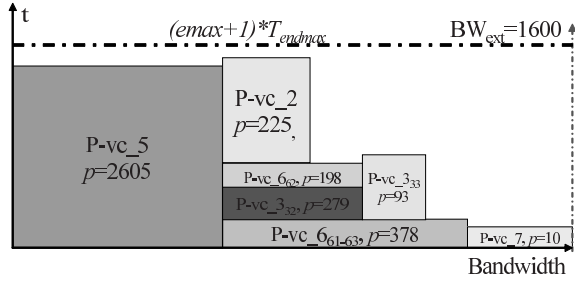


Fig. 6 Packing result when domain 2 is packed in step 4.

into the bin and L_M is updated as before. $dmax$ is a heuristic value (in %) which expresses how much t_{ipnew} can go over T_{endmax} . The algorithm repeats Step 3 until there is no available bandwidth and/or power or no suitable cubes can be found. If BW_{avail} and/or p_{avail} become zero, $curr_time$ is updated and the algorithm goes back to Step 1. If no suitable cubes were found, the algorithm proceeds to Step 4. For example, the ideal cube of domain no. 7 has $f_{ip} = 100$ MHz, $w_{ip} = 15$, $p_{ip} = 40$ and $t_{ip} = 0.10 \mu\text{sec}$. In Fig. 5, the idle bandwidth was 300 MHz and for $P\text{-vc}_7$, w_{ip} was first reduced to 3 at $f_{ip} = 100$ MHz. Consequently t_{ip} increased to $0.48 \mu\text{sec}$. While keeping t_{ip} constant, we are able to increase the w_{ip} to 12, while decreasing the shift frequency f_{ip} to 25 MHz and the power p_{ip} was lowered to 10 before packing the cube into the bin.

5.5 Step 4: Filling Idle Space by Decreasing Shift Frequency

Reaching Step 4 means that no cube satisfies p_{avail} . There is no choice but to lower the shift frequency of a $P\text{-vc}$ to fit the available idle space in the bin. The algorithm determines T_{endmax} and makes a copy of L_M called L_{tmp} . Then the shift frequencies of all cubes remaining in L_{tmp} are lowered until their power is less than or equal to p_{avail} . For each cube, the new scan-shift time t_{ipnew} is computed given a new bandwidth $BW_{ipnew} = BW_{avail}$. The shift frequency is halved and the virtual test bus is doubled to minimize power as long as t_{ipnew} remains constant. Similar to Step 3, the algorithm looks for a cube that satisfies $t_{ipnew} \leq T_{endmax} \times (1 + emax)$ and closest to T_{endmax} as we have found during experimentation that this gives better results than simply packing the first cube that satisfies the first condition. The cube is packed into the bin and L_M is updated as before. Step 4 is repeated until no cubes are found or until BW_{avail} and/or p_{avail} becomes zero. The algorithm again updates $curr_time$ and goes back to Step 1. Note that $emax$ is a heuristic value independent of $dmax$ which expresses how much t_{ipnew} can go over T_{endmax} . Steps 1 through 4 are repeated until L_M is empty. In Fig. 6, although there is a large BW_{avail} , p_{avail} is only 302 (see Fig. 7 (b)) so the f_{ip} of $P\text{-vc}_2$ is decreased to 50 MHz, and this leads to a decrease in $p_{ip} = 225$ while w_{ip} remained the same and t_{ip} doubled to $3.00 \mu\text{sec}$. Figure 7 shows the finished schedule separated into two 2-D graphs ((a)bandwidth vs. time and (b)power vs. time) to make it

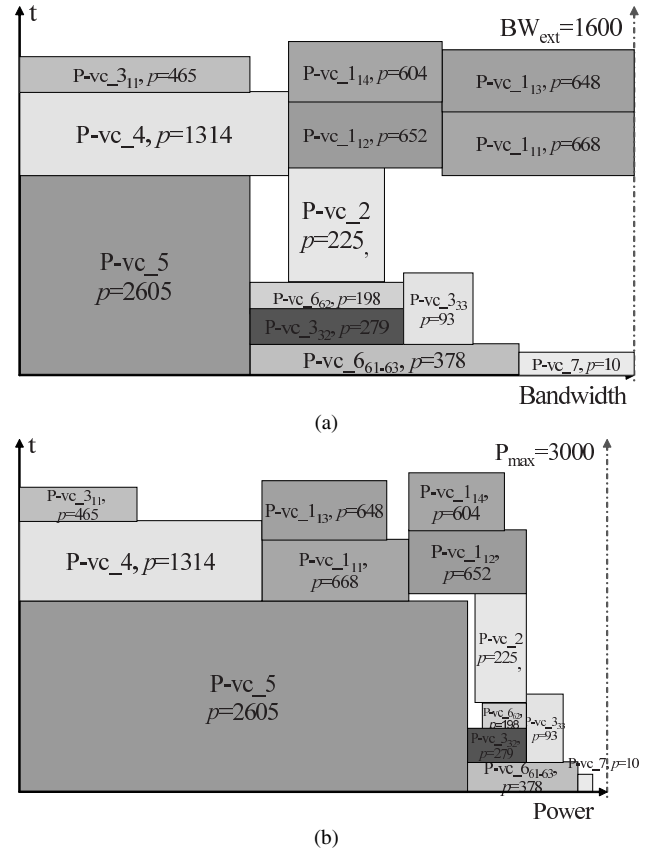


Fig. 7 Finished test schedule for hTCAD01 at $BW_{ext} = 1600$ (vs. time (a)) and $P_{max} = 3000$ (vs. time (b)).

easier to see that there are times when available bandwidth could not be utilized due to very low available power. Also note that by partitioning the clock domains, we increase the chance that a $P\text{-vc}$ can be scheduled (due to the presence of smaller cubes) during instances of low available power and/or bandwidth.

6. Experimental Result

The experiments were done using the benchmark multi-clock domain IP core *hTCAD01* which has seven clock domains, and we assumed that each domain can be further partitioned into sub-domains as shown in Table 1. In the table, $sd\#$ denotes the sub-domain number, f_{func} is the functional frequency, N_{in} , N_{out} , N_{bi} and N_{sc} are the number of inputs, outputs, bidirectional I/O and scan chains in the specific sub-domain respectively, L_{scij} is the length of each scan chain and P is the power dissipation of the sub-domains when shifting at 100 MHz and is made equal to the sum of all the scan chain lengths L_{scij} belonging to that sub-domain to simplify the setup.

The experiment was conducted under four different power constraints P_{max} : 1500, 3000, 4500 and ∞ . The maximum allowed frequency f_1 is 100 MHz, which is equal to f_{ATE} to synchronize the internal shift frequencies with the ATE. To see the effectiveness of the proposed method, the

Table 2 Comparison of scan-shift time for hCADT01 under various P_{max} .

(a) $P_{max} = 1500$.						(b) $P_{max} = 3000$.					
W_{ext}	T [9]	T [10]	T_{new}	%diff [9]	%diff [10]	W_{ext}	T [9]	T [10]	T_{new}	%diff [9]	%diff [10]
16	20.84	16.9	15.75	24.2	6.80	16	10.42	9.13	8.89	14.68	2.63
15	20.84	16.9	15.75	24.2	6.80	15	10.42	10.42	9.02	13.44	13.44
14	20.84	16.9	15.75	24.2	6.80	14	10.42	10.42	9.02	13.44	13.44
13	20.84	16.9	15.75	24.2	6.80	13	10.42	10.53	9.03	13.34	14.25
12	20.84	16.9	15.85	23.94	6.21	12	10.42	10.53	10.32	0.96	1.99
11	20.84	16.97	15.85	23.94	6.60	11	11.62	11.12	10.52	9.47	5.40
10	20.84	17.07	16.68	19.96	2.28	10	12.08	11.24	10.88	9.93	3.20
9	20.84	17.47	15.91	23.66	8.93	9	13.00	12.56	12.14	6.62	3.34
8	20.84	17.57	16.9	18.91	3.81	8	14.48	13.50	13.18	8.98	2.37
7	20.84	19.29	18.92	9.21	1.92	7	17.76	16.57	15.14	14.75	8.63
6	20.84	19.6	19.63	5.81	-0.15	6	20.84	17.19	17.19	17.51	0.00
5	25.04	23.38	23.19	7.39	0.81	5	23.24	21.81	20.64	11.19	5.36
4	29.76	26.16	25.34	14.85	3.13	4	29.76	26.15	25.52	14.25	2.41
3	41.68	34.06	34.08	18.23	-0.06	3	38.36	34.06	34.08	11.16	-0.06
2	59.88	51.61	50.81	15.15	1.55	2	58.02	50.36	50.48	13.00	-0.24
1	116.04	100.7	98.69	14.95	2.00	1	116.04	98.44	98.63	15.00	-0.19

(c) $P_{max} = 4500$.						(d) $P_{max} = \infty$.					
W_{ext}	T [9]	T [10]	T_{new}	%diff [9]	%diff [10]	W_{ext}	T [9]	T [10]	T_{new}	%diff [9]	%diff [10]
16	7.44	6.94	6.88	7.53	0.86	16	7.44	7.53	6.88	7.53	8.63
15	8.76	8.33	7.53	14.04	9.60	15	7.49	8.33	7.53	-0.53	9.60
14	8.88	8.79	7.81	12.05	11.15	14	8.88	8.79	7.81	12.05	11.15
13	10.42	8.93	8.53	18.14	4.48	13	9.59	8.79	8.53	11.05	2.96
12	10.42	9.75	9.44	9.40	3.18	12	10.42	9.15	9.44	9.40	-3.17
11	10.42	9.75	10.18	2.30	-4.41	11	10.42	9.75	10.18	2.30	-4.41
10	11.62	10.58	11.2	3.61	-5.86	10	11.62	10.58	11.2	3.61	-5.86
9	12.78	11.85	11.85	7.28	0.00	9	12.78	11.83	11.85	7.28	-0.17
8	14.88	13.50	13.36	10.22	1.04	8	14.88	13.5	13.36	10.22	1.04
7	15.63	15.43	15.09	3.45	2.20	7	15.63	15.43	15.09	3.45	2.20
6	19.20	17.19	17.19	10.47	0.00	6	19.18	17.19	17.19	10.38	0.00
5	23.24	21.81	20.64	11.19	5.36	5	23.24	21.81	20.64	11.19	5.36
4	29.01	26.15	25.52	12.03	2.41	4	29.01	24.84	25.52	12.03	-2.74
3	38.36	34.06	34.08	11.16	-0.06	3	38.36	34.06	34.08	11.16	-0.06
2	58.02	50.36	50.48	13.00	-0.24	2	58.02	50.36	50.48	13.00	-0.24
1	116.04	98.44	98.63	15.00	-0.19	1	116.04	98.44	98.63	15.00	-0.19

resulting shift times denoted by T_{new} are compared to the results from [9], marked T [9], and from [10], marked T [10], in Table 2. All times are in microseconds. %diff [9] and %diff [10] are the differences in percentage with respect to [9] and [10] respectively. During the experiments, d_{max} and e_{max} were independently varied from 0% to 200% to find the optimal combination that yields a minimum scan-shift time. The experiments were done using a Sun Fire V490 1.35 GHz UltraSPARC IV workstation with 32 GB memory and the 40,000 looped reruns of the program didn't take more than 1 sec. of CPU time.

At the tightest power constraint of $P_{max} = 1500$, our algorithm was able to decrease the shift time with a maximum of 24.42% compared to [9]. The average gain in test time, as P_{max} is decreased, increases dramatically from 8.69% at $P_{max} = \infty$ to 18.36% at $P_{max} = 1500$. This can be attributed to the fact that wider W_{ext} and lower P_{max} makes partitioning the domains more effective because of the extra freedom it gives during scheduling. Compared to [10], the trend is different and there is an almost constant average

gain of around 4% across all power constraints and a maximum gain of 14.25% at $P_{max} = 3000$. Small differences in time (0-1%) are attributed to discrepancies in rounding-off among the programs used and makes them negligible, so our algorithm matches or exceeds [10] in 90% of the cases.

In [8], [9], the area increase due to the demultiplexing-multiplexing circuitry, scan-control modules and other necessary logic to implement the multi-clock domain wrapper was stated to be less than 10% the area size taken by the IEEE 1500 wrapper and other scan logic. Since our approach only requires a slight modification of the scan control circuitry in [8], [9], it is safe to assume that the added overhead would be minimal. Furthermore, as manufacturing processes become smaller and transistor count becomes higher, the probable DFT overhead becomes more and more negligible in light of the possible gains in test application time. Also, the added flexibility of domain partitioning and partitioned test scheduling would be of greater benefit as designers start to re-use older generation multi-clock domain circuits as IP-cores in newer, more complex designs.

7. Conclusion

We have presented a novel method of designing a test wrapper for multi-clock domain cores by effectively utilizing clock domain partitioning, bandwidth matching and gated-clocks. With minimal hardware overhead for gated-clock control, we have dramatically improved upon earlier methods which concurrently activate all the domains during test, especially under tight power constraints. Overall, the division of clock domains enabled us to give better results than all the previous methods with comparable area overhead.

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