

# A New Class of Sequential Circuits with Combinational Test Generation Complexity

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**Abstract**—We introduce a new class of sequential circuits with combinational test generation complexity which we call *internally balanced* structures. It is shown that sequential circuits can be classified by their structure as follows: {sequential circuits of acyclic structure}  $\supset$  {sequential circuits of internally balanced structure}  $\supset$  {sequential circuits of balanced structure} and that internally balanced structures allow test generation with combinational test generation complexity. On the other hand, if finite state machines (FSMs) are classified by their realization possibility, it can be shown that {FSMs which can be realized as a sequential circuit of acyclic structure} = {FSMs which can be realized as a sequential circuit of internally balanced structure}  $\supset$  {FSMs which can be realized as a sequential circuit of balanced structure}. Hence, any FSM realizable with acyclic structure can be also realized with internally balanced structure which allows test generation with combinational test generation complexity. In addition, we discuss the definition of test generation possibility with combinational test generation complexity and introduce a new definition which covers the previous narrow definition. Finally, we study applications to design for testability based on the partial scan and to test generation time reduction for sequential circuits in general, using characteristics of the internally balanced structures. The experimental results shows the effectiveness of this approach.

**Index Terms**—Balanced structure, complexity, design for testability, partial scan, reducibility, sequential circuits, test generation.

## 1 INTRODUCTION

TEST generation for a sequential circuit is, in general, a difficult and intractable task which may be unsolvable within a reasonable time for a large-scale circuit [1], [2]. Methods of solution include *design for testability*, like the scan design method, in which some or all of the flip-flops are replaced with scan flip-flops so that they are chained into a shift register during test mode and, hence, they can be directly controlled and observed [1], [2]. When all the flip-flops of a circuit are replaced with scan flip-flops (*full scan design*), all the scan flip-flops are treated as equivalents to external I/O terminals and, hence, the test generation can be performed for the remaining circuit (called the “kernel circuit”) with the exclusion of all flip-flops, i.e., for the combinational part of the sequential circuit. Therefore, the full scan design method can reduce the test generation problem for a sequential circuit to the problem of test generation for a combinational circuit.

If the test generation problem for a sequential circuit can be reduced to the problem of test generation for a combinational circuit where all the flip-flops of the sequential circuit can be replaced by wires, then such a sequential circuit is called a sequential circuit allowing test generation with combinational test generation complexity or, simply, a *sequential circuit with combinational test generation complexity*, and this transformation is called *combinational transformation (C-transformation)*. For example, *balanced structures* [3] are one class of circuit structures with this feature. A sequential circuit is a balanced structure if,

for any pair of primary input and primary output, all paths between them have the same number of flip-flops. In [4], a subclass of balanced structure, called *strongly balanced structures*, is introduced.

In this paper, we shall first introduce an *extended combinational transformation (C\*-transformation)* and a wider class of sequential circuits with combinational test generation complexity which we call *internally balanced structures*. It is shown that sequential circuits can be classified by their structure as follows: {sequential circuits of acyclic structure}  $\supset$  {sequential circuits of internally balanced structure}  $\supset$  {sequential circuits of balanced structure}. Sequential circuits of acyclic structure do not necessarily allow test generation with combinational test generation complexity. However, it can be shown that sequential circuits of internally balanced structure allow test generation with combinational test generation complexity as well as balanced structure. On the other hand, if finite state machines (FSMs) are classified by their realization possibility, it can be shown that {FSMs which can be realized as a sequential circuit of acyclic structure} = {FSMs which can be realized as a sequential circuit of internally balanced structure}  $\supset$  {FSMs which can be realized as a sequential circuit of balanced structure}. From this result, we can see that any FSM realizable with acyclic structure can be also realized with internally balanced structure which is capable of test generation with combinational test generation complexity. In addition, in this paper, we shall discuss the definition of test generation possibility with combinational test generation complexity and introduce a new definition which covers the narrow definition by [3]. Finally, we shall study applications to design for testability based on the partial scan and to test generation time reduction for sequential circuits in general, using characteristics of the

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Manuscript received 16 June 1999; accepted 18 July 2000.  
For information on obtaining reprints of this article, please send e-mail to: tc@computer.org, and reference IEEECS Log Number 110077.

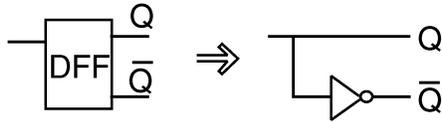


Fig. 1. Deletion of flip-flops.

internally balanced structures. The experimental results shows the effectiveness of this approach.

## 2 SEQUENTIAL CIRCUITS WITH COMBINATIONAL TEST GENERATION COMPLEXITY

A sequential circuit with combinational test generation complexity must be a circuit without feedback, i.e., of acyclic structure. Therefore, we shall first limit the subject to sequential circuits of acyclic structure. Further, for simplicity, we shall limit flip-flops (referred to hereafter as FFs) to DFFs. Other kinds of FF can be handled similarly by replacing the FF with a circuit composed of DFF and extra logic that is functionally equivalent to the original FF, e.g., an FF with a hold input can be handled by replacing it with a DFF and a multiplexer with feedback.

At a fanout point, the signal line at the input side is called *the fanout stem* and the signal lines at the output side are called *fanout branches*. The number of FFs included in a path is called the *sequential depth* of the path. The largest sequential depth over the paths from the primary inputs of a sequential circuit to its primary outputs is regarded as the sequential depth of the sequential circuit. Suppose  $x$  is a primary input and  $x_i$  and  $x_j$  are branches of  $x$ . If no path exists such that a primary output  $z_k$  can be reached from  $x_i$  and  $x_j$  over equal depth paths, then  $x_i$  and  $x_j$  are called *separable*.

A set composed of subsets of a state set  $Q$  is called a *decomposition* of  $Q$ , with each subset constituting a block. A decomposition whose blocks are mutually disjoint is called a *partition*. For a decomposition  $\Pi = \{B_1, B_2, \dots, B_k\}$ , where the blocks are denoted by  $B_i$  and inputs by  $I_j$ , if the state set obtained by transition at each input  $I_j$  from the state belonging to  $B_i$  is denoted by  $B_{ij}$ , then decomposition composed of blocks  $B_{ij}$  will be expressed by  $m(\Pi)$ . If  $Q$  itself is considered a partition, then it is expressed by  $I$  and, in addition, a partition with each block constituting one state is expressed by  $O$ .

**Combinational Transformation (C-Transformation):** Given a sequential circuit  $S$  of acyclic structure, we define its combinational equivalent  $C(S)$  as the combinational circuit formed by replacing each FF in  $S$  by a wire (for the case of negative FF output, a NOT gate is added, see Fig. 1).

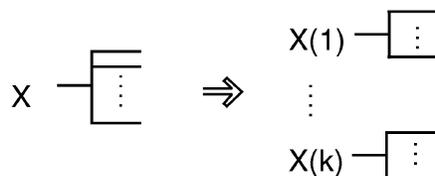
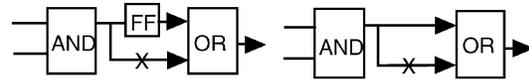


Fig. 2. Primary input separation.



s-a-0 (detectable fault)      s-a-0 (redundant fault)

Fig. 3. Circuit example and  $C^*$ -transformation.

Such a transformation is called the combinational transformation (*C-transformation*).

**Extended Combinational Transformation ( $C^*$ -Transformation):** A transformation based on the following two operations with a sequential circuit  $S$  of acyclic structure is called the extended combinational transformation ( *$C^*$ -transformation*), and the resulting combinational circuit is denoted by  $C^*(S)$ .

1. For a primary input with fanout branches, the set of fanout branches of that primary input is denoted by  $X$ . Let us obtain the smallest partition of  $X$  which satisfies the following statement: If branches  $x_i$  and  $x_j$  belong to different blocks  $X(i), X(j)$  of partition  $\Pi$  ( $x_i \in X(i), x_j \in X(j), X(i) \neq X(j)$ ), then  $x_i$  and  $x_j$  are separable. As shown in Fig. 2, each partitioned block is provided with a new primary input separated from the original primary input. (Note: While separating the primary inputs, branch faults are treated as a multiple fault present simultaneously in all these branches.)
2. FFs are replaced by wires, as illustrated in Fig. 1.

**Possibility of test generation with combinational test generation complexity:** If it is true that, by assuming  $S$  denotes an acyclic sequential circuit and  $C^*(S)$  denotes the  $C^*$ -transformed combinational circuit, the necessary and sufficient condition for testing a fault  $f$  in  $S$  is that the fault  $f_c$  in  $C^*(S)$  corresponding to  $f$  can be tested in  $C^*(S)$ , then the sequential circuit  $S$  allows test generation with combinational test generation complexity. Such a sequential circuit is called a *sequential circuit allowing test generation with combinational test generation complexity* or, simply, a *sequential circuit with combinational test generation complexity*.

**Acyclic Structure:** When a sequential circuit  $S$  does not contain any closed path,  $S$  is regarded as an acyclic structure.

Even an acyclic circuit may not necessarily allow test generation with combinational test generation complexity. Fig. 3 shows an example of such a circuit.

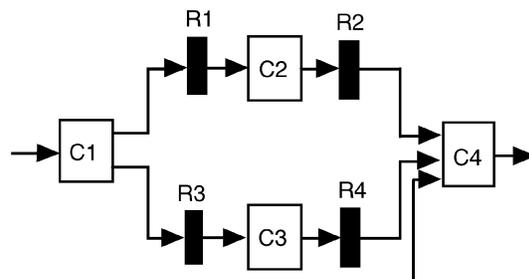


Fig. 4. Example of balanced structure.

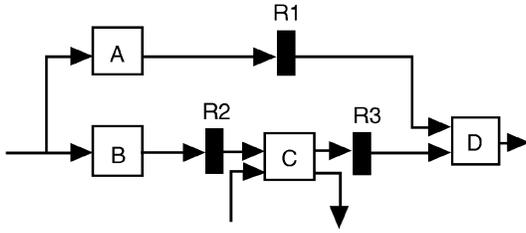


Fig. 5. Example of internally balanced structure.

**Balanced Structure** [3]: If, for any pair of primary input and primary output in a circuit S, the sequential depths of all paths connecting these two points are equal, then S is regarded as a balanced structure. Therefore, since in a sequential circuit of balanced structure none of its primary inputs is separable, the C\*-transformation is performed only by operation (2) and, hence,  $C^*(S) = C(S)$  (see Fig. 4).

**Internally Balanced Structure:** If a circuit  $S^*$  resulting from operation 1 of the C\*-transformation on a circuit S is a balanced structure, then S is regarded as an internally balanced structure.

The circuit shown in Fig. 5 is an internally balanced structure but is not a balanced structure. The relation among three structures is shown in Fig. 6.

**Theorem 1** [5]. *The necessary and sufficient condition for realization of an FSM M as an acyclic structure is  $m^k(I) = O$  for some constant, where  $m^k(I)$  is inductively defined as  $m^1(I) = m(I)$  and  $m^k(I) = m(m^{k-1}(I))$  for  $k > 1$ .*

**Lemma 1.** *The statement that an FSM M is expressed as  $m^k(I) = O$  for any k is equivalent to the statement that M can be realized by a finite input memory machine of length k (see Fig. 7). In addition, it is equivalent to the statement that any input sequence of length k becomes a synchronizing sequence [1] of M.*

Therefore, we can obtain the following corollary.

**Corollary 1.** *The necessary and sufficient condition for realization of an FSM M as an acyclic structure is that M can be realized by a finite input memory machine.*

Proofs of Theorem 1 and Corollary 1 are given in [5]. A different proof can be done by using the following Lemma 2 and Corollary 2.

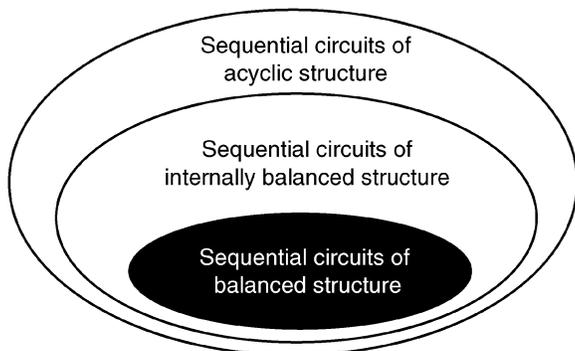


Fig. 6. Classification of sequential circuits by structure.

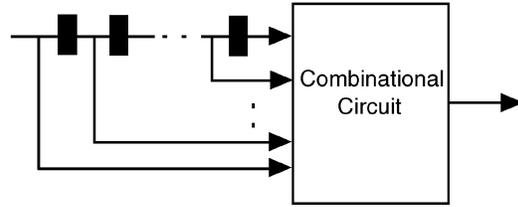


Fig. 7. Finite input memory realization.

**Lemma 2.** *Any sequential circuit of acyclic structure (Fig. 8) can be transformed into an equivalent circuit allowing realization with a finite input memory, by operations of retiming (Fig. 9) and logic duplication (Fig. 10).*

**Theorem 2.** *Any FSM allowing realization as an acyclic structure can be realized as an internally balanced structure.*

**Proof.** A circuit allowing realization by a finite input memory (Fig. 7) can be transformed into an equivalent circuit of the type shown in Fig. 11 by retiming. This statement and Corollary 1 (or Lemma 2) constitute a theorem. □

**Theorem 3.** *An FSM exists which can be realized as an acyclic structure, but which cannot be realized as a balanced structure.*

**Proof.** If, for any input x, an output z varies depending on the values of x in different time frames, then, for the circuit realizing z, a number of paths exist which are characterized by different sequential depths required to reach z from x. Therefore, it cannot be realized as a balanced structure. □

For example, in Fig. 12, output is determined by input x in the current time frame and by input x at some previous time frame. Therefore, there are two paths of different depth leading from x to z.

From Theorems 2 and 3 we can conclude the following (see Fig. 13):

{FSMs which can be realized as a sequential circuit of acyclic structure} = {FSM which can be realized as a finite input memory machine} = {FSMs which can be realized as a sequential circuit of internally balanced structure}  $\supset$  {FSMs which can be realized as a sequential circuit of balanced structure}.

### 3 TEST GENERATION COMPLEXITY

#### 3.1 Acyclic Structure

Fig. 14a illustrates an example of a sequential circuit with acyclic structure. For this circuit, the test pattern can be obtained by applying the test generation algorithm for combinational circuits to the time-expanded combinational

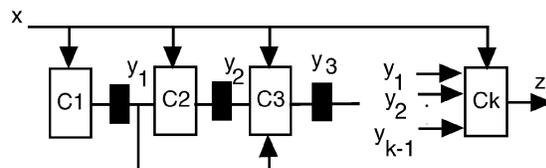


Fig. 8. General acyclic structure.

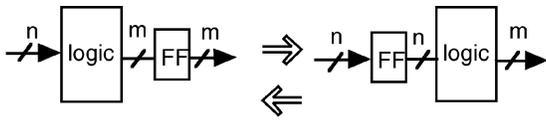


Fig. 9. Retiming.

circuit illustrated in Fig. 14b. Since there are several subcircuit duplicates, we must consider the same fault in each subcircuit, i.e., a kind of multiple faults. Assuming a sequential depth  $d$ , the time-expanded circuit will include in the worst case  $d + 1$  subcircuit duplicates. After obtaining the test pattern for the time-expanded combinational circuit, we can generate a test sequence (for the sequential circuit) corresponding to the test pattern. The length of the test sequence is  $d + 1$  in worst case.

### 3.2 Balanced Structure

**Theorem 4 [3].** *If a sequential circuit  $S$  is a balanced structure,  $S$  allows test generation with combinational test generation complexity.*

The sequential circuit  $S$  shown in Fig. 4 is a balanced structure. Replacing all flip-flops in  $S$  by wires, a combinational circuit  $C(S)$ , as shown in Fig. 15, is obtained. The test pattern is obtained by applying to this combinational circuit a combinational test generation algorithm (ATG). From the test pattern generated by the combinational ATG, we obtain the corresponding test sequence, taking time into account. Assuming a sequential depth  $d$ , the length of the test sequence is  $d + 1$  in worst case. In this test sequence, the same input values are applied to each primary input during  $d + 1$  clocks.

An advantage of the sequential circuit with balanced structure is that it has time expansion to  $d + 1$ , similarly for the acyclic structure, but there are no duplicates in the time-expanded circuit.

### 3.3 Internally Balanced Structure

**Theorem 5.** *If a sequential circuit  $S$  is an internally balanced structure,  $S$  allows test generation with combinational test generation complexity.*

**Proof.** First, we shall prove that if a fault  $f$  in  $S$  can be tested, then the fault  $f_c$  in  $C^*(S)$  corresponding to  $f$  can be tested

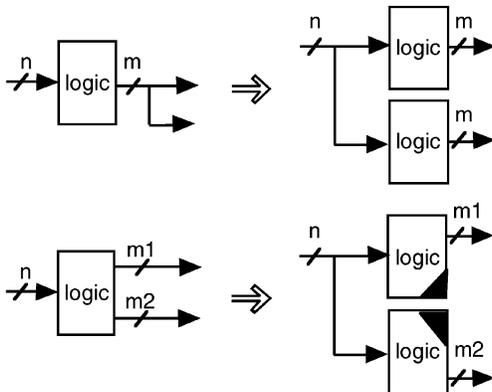


Fig. 10. Logic duplication.

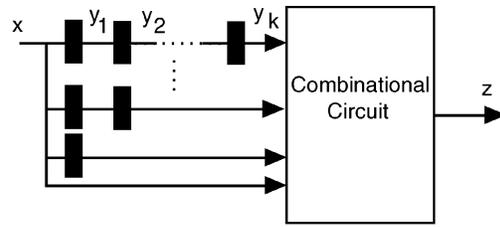


Fig. 11. Internally balanced structure.

in  $C^*(S)$ . It is sufficient to prove that a test pattern  $T_c$  for  $f_c$  in  $C^*(S)$  can be generated from the test sequence  $T$  for  $f$  in  $S$ . Here, we shall treat a fault at a primary input with fanout as a multiple fault which exits simultaneously in all the fanout branches of the input.

If the sequential depth of  $S$  is  $d$ , the length of  $T$  is  $d + 1$ . Assume that  $f$  can be detected in a time frame  $t$  at primary output  $z_k$  ( $1 < t < d + 1$ ). From this test sequence  $T$ , we can define the primary input value  $x_i$  in  $C^*(S)$  for the test pattern  $T_c$ , as shown below.

1. Case of  $x_i$  not being a primary input resulting from separation:

The sequential depth from  $x_i$  to  $z_k$  is uniquely determined. Let the depth be  $d_{ik}$ . The value of  $x_i$  required to detect  $f$  in  $T$  at  $z_k$  is the value of the primary input  $x_i$  in time frame  $t - d_{ik}$ . Therefore, the primary input value  $x_i$  in time frame  $t - d_{ik}$  in  $T$  can be set to define the primary input value  $x_i$  of the test pattern  $T_c$ .

2. Case of  $x_i$  being a primary input resulting from separation:

Suppose that the original primary input value of  $x_i$  in  $S$  is denoted  $x$ . Although  $x$  is a primary input in  $S$ ,  $x_i$  is not a primary input. In  $C^*(S)$ ,  $x_i$  is a primary input. Since this is the case of an internally balanced structure, we can uniquely determine the sequential depth from  $x_i$  to  $z_k$ , which is denoted as  $d_{ik}$ . The value of  $x_i$  required to detect  $f$  in  $T$  at  $z_k$  equals the  $x$  value in time frame  $t - d_{ik}$ . The  $x$  value in time frame  $t - d_{ik}$  in  $T$  is set to define the primary input value  $x_i$  in the test pattern  $T_c$ .

It is evident that the test pattern  $T_c$  defined as described above will detect the fault  $f_c$  in  $C^*(S)$ . Next, we prove that if the fault  $f_c$  in  $C^*(S)$  can be tested, then the fault  $f$  in  $S$  corresponding to  $f_c$  can be tested in  $S$ . It is sufficient to prove that the test sequence  $T$  for  $f$  in  $S$  can be generated from the test pattern  $T_c$  in  $C^*(S)$ . Suppose  $f_c$  can be detected at the primary output  $z_k$  in the test pattern  $T_c$ . The primary input value  $x_i$  of the test sequence  $T$  such that the fault  $f$  corresponding to  $f_c$  can

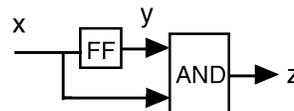


Fig. 12. Circuit example.

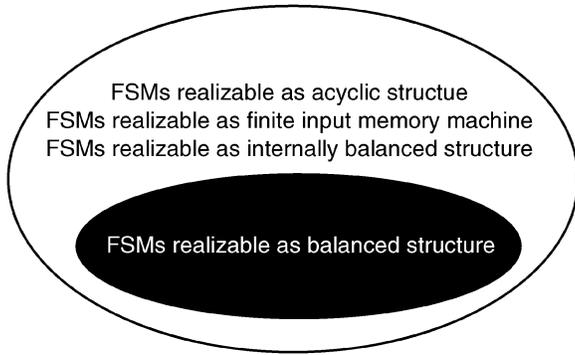


Fig. 13. Classification of finite state machines.

be detected at the primary output  $z_k$  in time frame  $t$  is determined as follows:

1. Case of  $x_i$  not being a primary input resulting from separation:  
 The sequential depth from  $x_i$  to  $z_k$  is uniquely determined. Let the depth be  $d_{ik}$ . The primary input value in the test pattern  $T_c$  is set to the primary input value  $x_i$  at the time frame  $t - d_{ik}$  of the test sequence  $T$ .
2. Case of  $x_i$  being a primary input resulting from separation:  
 Assume that the primary input  $x_i$  in  $S$  was separated to obtain the primary inputs  $x_{i1}, x_{i2}, \dots, x_{in}$  in  $C^*(S)$ . Since this is the case of an internally balanced structure, we can uniquely determine each sequential depth from  $x_{ij}$  to  $z_k$ , which is denoted by  $d_{ijk}$ . Since these are separable, all  $d_{ijk}$  ( $j = 1, 2, \dots, n$ ) are different sequential depths. Therefore, all time frames ( $t - d_{ijk}$ ) ( $j = 1, 2, \dots, n$ ) are different, and can be set to  $n$  time frames in the test sequence  $T$  as described below. That is, the primary input values  $x_{ij}$  ( $j = 1, 2, \dots, n$ ) of test pattern  $T_c$  are set to define

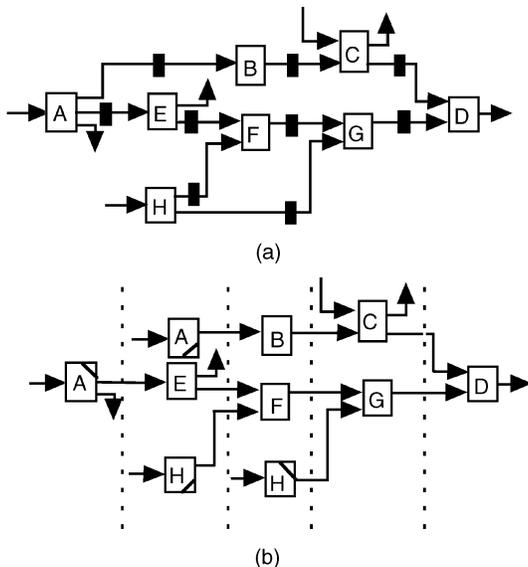


Fig. 14. (a) Acyclic structure, and (b) time expansion.

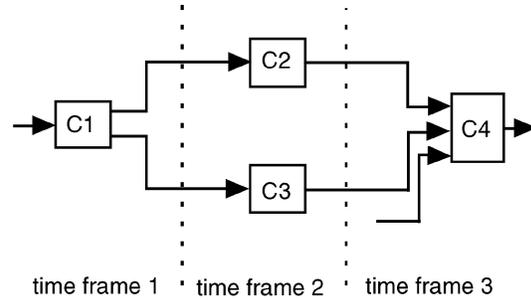


Fig. 15. C-transformed combinational circuit  $C(S)$ .

the primary input value  $x_i$  in time frames ( $t - d_{ijk}$ ) ( $j = 1, 2, \dots, n$ ) in the test sequence  $T$ .

It is evident that the test sequence  $T$  defined above can detect the fault  $f$  in  $S$ .  $\square$

In Fig. 5, consider the  $C^*$ -transformation of the sequential circuit  $S$  with internally balanced structure. Since in  $S$  the input fanout branches which are fanned out at primary input  $x_1$  are separable, we separate them. Then, on replacing the flip-flops by wires, we obtain the combinational circuit  $C^*(S)$  as shown in Fig. 16.

We can then obtain the test pattern for each fault in this  $C^*$ -transformed combinational circuit by using a combinational ATG. Taking the time frame into account, we can construct the test sequence for the original sequential circuit. Assuming that the sequential depth of the circuit is  $d$ , the length of the test sequence is  $d + 1$  at most.

An advantage of sequential circuits with internally balanced structure is that there are no duplicates in the circuit which was time expanded to  $d + 1$ , similarly for the case of balanced structures.

We have introduced a new class of sequential circuits (internally balanced structures) with combinational test generation complexity (Theorem 5) which is larger than the class of sequential circuits of balanced structure. On the other hand, sequential circuits of acyclic structure do not necessarily allow test generation with combinational test generation complexity as illustrated in Fig. 3. From Theorem 3, it is not always possible for an FSM realizable as acyclic structure to be realized as balanced structure. However, from Corollary 2, any FSM realizable as acyclic structure can be also realized as internally balanced structure. Therefore, any sequential circuit of acyclic structure can be transformed or modified into an function-equivalent sequential circuit of internally balanced

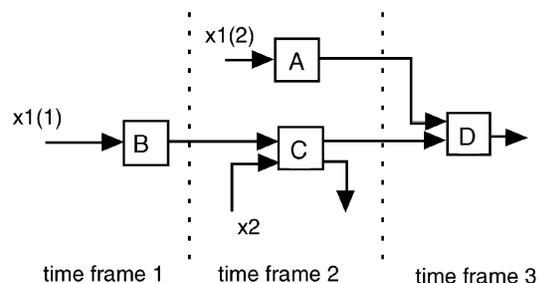


Fig. 16.  $C^*$ -transformed circuit  $C^*(S)$ .

structure which is capable of test generation with combinational test generation complexity. In this sense, the class of sequential circuits of internally balanced structure might be one of the largest classes of sequential circuits with combinational test generation complexity.

#### 4 NEW DEFINITION OF POSSIBILITY OF TEST GENERATION WITH COMBINATIONAL TEST GENERATION COMPLEXITY

In [3], the possibility of test generation with combinational test generation complexity was defined as follows: If the test generation problem for  $S$  can be reduced to the test generation problem of  $C$ -transformed combinational equivalent  $C(S)$ , the sequential circuit  $S$  is said to be in a class of sequential circuits with combinational test generation complexity. In Section 2, we extended the definition of possibility of test generation with combinational test generation complexity by introducing an extended combinational transformation ( $C^*$ -transformation).

Here, we shall further extend the concept and introduce a new definition of the possibility of test generation with combinational test generation complexity by extending those transformations.

##### $P_c$ : Combinational Test Generation Problem

Instance: A combinational circuit  $C$  and a fault  $f$ .

Question: Is there a test pattern to detect  $f$  in  $C$ ?

##### $P_s$ : Sequential Test Generation Problem

Instance: A sequential circuit  $S$  and a fault  $f$ .

Question: Is there a test sequence to detect  $f$  in  $S$ ?

##### $P_\alpha$ : Class $\alpha$ Test Generation Problem

Instance: A sequential circuit  $S$  in  $\alpha$  and a fault  $f$ .

Question: Is there a test sequence to detect  $f$  in  $S$ ?

Let  $T_c(n)$  and  $T_\alpha(n)$  be the time complexity of test generation problems  $P_c$  and  $P_\alpha$ , respectively, where  $n$  is the size of a problem instance.

**Reducibility:** Problem  $A$  is *reducible* to problem  $B$  if there exists a transformation such that, for any instance  $a \in A$ , the solution of  $a$  is the same as the solution of  $\tau(a) \in B$ .

##### Combinational Test Generation Complexity:

A class of sequential circuits,  $\alpha$ , is called to have *combinational test generation complexity* if there exists a transformation  $\tau$  such that

1.  $P_\alpha$  is reducible to  $P_c$  by transformation  $\tau$ , and
2. for each  $S \in \alpha$ ,  $T_\tau(\text{size of } S) \leq T_c(\text{size of } S)$  and  $T_c(\text{size of } \tau(S)) \leq T_c(\text{size of } S)$ , where  $T_\tau$  is the time complexity of transformation  $\tau$ .

From this definition,

$$T_\tau(\text{size of } S) + T_c(\text{size of } \tau(S)) \leq T_c(\text{size of } S).$$

Therefore, the test generation problem of a sequential circuit  $S$  with combinational test generation complexity can be solved by first transforming  $S$  to  $\tau(S)$  and then applying a combinational ATG to the transformed combinational circuit  $\tau(S)$ . The total time complexity is less than  $T_c(\text{size of } S)$ , i.e., the time complexity of combinational test generation problem.

As for the complexity of transformation  $T_\tau$ , it must be less than the combinational test generation complexity  $T_c$ .

However, by reason of the NP-completeness of the combinational test generation problem  $P_c$ , if one considers  $T_c$  might be  $O(2^N)$  in worst case, where  $N$  is the number of inputs of the circuit, then almost all circuits are in the class of sequential circuits with combinational test generation complexity, and our discussion becomes meaningless. Fortunately, it is known that  $T_c$  seems to be  $O(n^k)$  for some constant  $k$  (less than 2) empirically, where  $n$  is the number of gates in the circuit. Therefore, when we devise a new transformation method to further expand the class of sequential circuits with combinational test generation complexity, we could consider  $T$  to be less than  $O(n^k)$  for practical use. In the next section, we shall reconsider each test generation complexity for each class of acyclic, internally balanced, and balanced structures under the assumption of  $T_c = O(n^k)$  for some constant  $k$ .

### 5 TEST GENERATION COMPLEXITY UNDER

$$T_c = O(n^k)$$

#### 5.1 Balanced Structure

Let  $\beta$  be the class of sequential circuits of balanced structure. By repeating retiming operations shown in Fig. 9, any sequential circuit  $S \in \beta$  can be transformed into a combinational circuit equivalent to  $C(S)$  (Fig. 17 illustrates this). Obviously,  $P_\beta$  is reducible to  $P_c$  by this transformation  $\tau$ . Let  $n$  be the size of  $S$  or the number of wires in  $S$ , then the size of  $\tau(S)$  becomes  $O(n)$ . We can easily see that the time complexity of this transformation is also  $O(n)$ . Hence, for each  $S \in \beta$ ,  $T_\tau(\text{size of } S) \leq T_c(\text{size of } S)$  and  $T_c(\text{size of } \tau(S)) \leq T_c(\text{size of } S)$ . Therefore, the class of sequential circuits of balanced structure has the combinational test generation complexity.

#### 5.2 Internally Balanced Structure

Let  $\gamma$  be the class of sequential circuits of internally balanced structure. By repeating retiming operations in Fig. 9, any sequential circuit  $S \in \gamma$  can be transformed into a finite input memory realization form in Fig. 11 whose combinational part is equivalent to  $C^*(S)$ . Fig. 18 illustrates this. (Note that, in Fig. 18, the timing of the output of borrowed FFs is just one clock before the timing of the output of the  $C^*$ -transformed circuit.) In the same way as the proof of Theorem 5, we can show that  $P_\gamma$  is reducible to  $P_c$  by this transformation  $\tau$ . Let  $n$  be the size of  $S$  or the number of wires in  $S$ , then the size of  $\tau(S)$  is also  $O(n)$ . We can see that the time complexity of this transformation is  $O(n^{k_1})$  for some constant  $k_1$ . Suppose  $T_c(n) = O(n^k)$  for some constant  $k$  such that  $k_1 \leq k$ . Then, we have  $T_\tau(n) \leq T_c(n)$  and, hence, for each  $S \in \gamma$ ,  $T_\tau(\text{size of } S) \leq T_c(\text{size of } S)$  and  $T_c(\text{size of } \tau(S)) \leq T_c(\text{size of } S)$ . Therefore, the class of sequential circuits of internally balanced structure has the combinational test generation complexity.

#### 5.3 Acyclic Structure

Let  $\alpha$  be the class of sequential circuits of acyclic structure. By repeating the retiming operation (Fig. 9) and logic duplication operation (Fig. 10), any sequential circuit  $S \in \alpha$  can be transformed into a sequential circuit of a finite input memory realization form shown in Fig. 11 whose combinational part is equivalent to  $C^*(S)$  (Fig. 14 illustrates this).

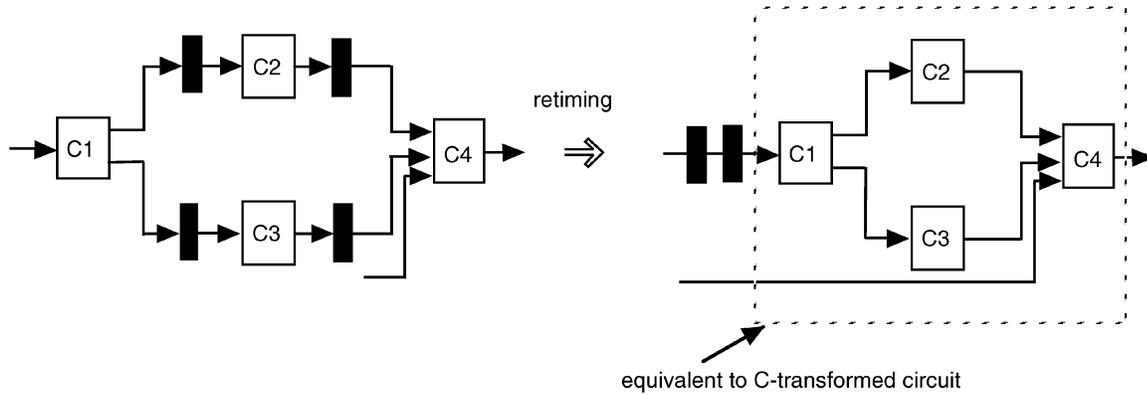


Fig. 17. Balanced structure and transformation by retiming.

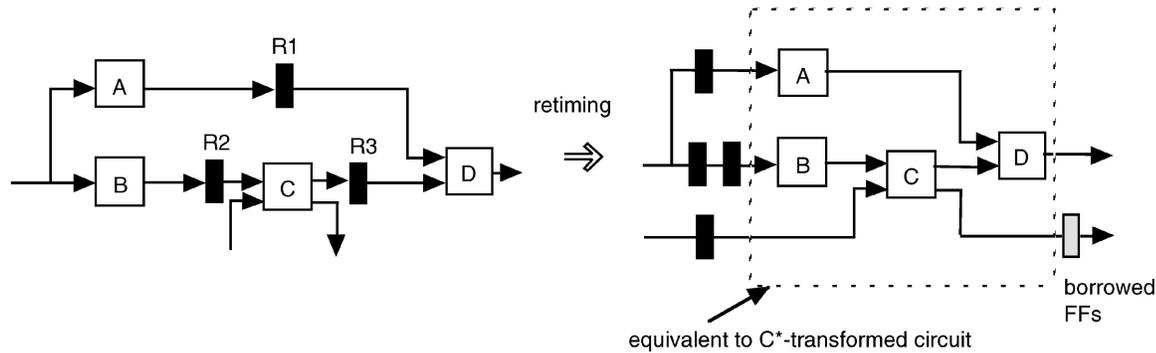


Fig. 18. Internally balanced structure and transformation by retiming.

However, due to logic duplication, the size of transformed circuit  $\tau(S)$  increases and is  $O(n^{k_2})$  for some constant  $k_2 > 1$ . Suppose  $T_\tau(n) = O(n^{k_1})$  and  $T_c(n) = O(n^k)$  for some constants  $k_1$  and  $k$ , and  $k_1 \leq k$ . We can see  $T_\tau(\text{size of } S) \leq T_c(\text{size of } S)$ . However,

$$T_c(\text{size of } \tau(S)) = T_c(n^{k_2}) = O(n^{k_2 k}) > O(n^k) = T_c(\text{size of } S).$$

Therefore, we cannot say that the class of sequential circuits of acyclic structure has the combinational test generation complexity.

From the above discussion, the acyclic structure that is neither internally balanced nor balanced is not good in the sense that it does not have the combinational test generation complexity. However, as shown in Lemma 2 and Corollaries 1 and 2 in Section 2, any acyclic structure can be transformed or modified into internally balanced structure. Therefore, the internally balanced structure is one of the best or the widest class of sequential circuits that has the combinational test generation complexity.

## 6 APPLICATION TO SEQUENTIAL CIRCUITS IN GENERAL

### 6.1 Kernel Circuit

The above discussion concerned acyclic sequential circuits (without feedback). We shall now consider the general case of sequential circuits (with feedback). Suppose that FFs are somehow partitioned into two parts, one called internal FFs, and the other external FFs, as illustrated in Fig. 19. In addition, the circuit part remaining upon exclusion of the external FFs from the sequential circuit is called the "kernel

circuit." The kernel circuit input can be divided into the original primary input of the circuit and pseudo-input from the external FF. The kernel circuit output can be divided into the primary output and the pseudo-output.

### 6.2 Problem of Kernel Circuit Extraction

Consider the problem of extracting the kernel circuits from acyclic/balanced/internally balanced structures by selecting the minimum number of external FFs from any sequential circuit.

**Acyclic Structure:** A method for selecting minimal number of external FFs to form acyclic structure is in [7].

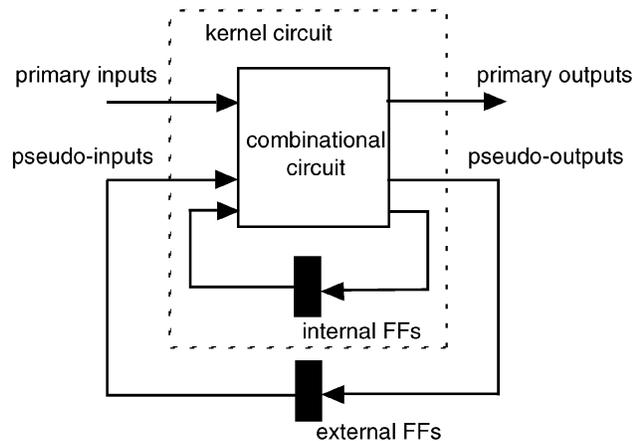


Fig. 19. Kernel circuit.

TABLE 1  
Circuit Characteristics

	Number of inputs	Number of outputs	Number of nets	Total number of FFs	Number of external FFs	Number of internal FFs	Sequential depth
Circuit 1	24	8	3780	48	16	32	2
Circuit 2	24	32	7966	48	16	32	2

TABLE 2  
Circuit 1

	Fault coverage	Fault efficiency	Number of test patterns	Test sequence length	Test generation time
non scan	77.99%	93.04%	-----	200	3369 sec
full scan	85.29%	99.99%	48	2400	19 sec
this method	84.99%	99.31%	39	757	404 sec

TABLE 3  
Circuit 2

	Fault coverage	Fault efficiency	Number of test patterns	Test sequence length	Test generation time
non scan	49.28%	65.67%	-----	59	31,815 sec
full scan	83.91%	99.98%	68	3380	57 sec
this method	83.85%	99.73%	59	1137	445 sec

**Balanced Structure:** A method for selecting minimal number of external FFs to form a balanced structure is in [3].

**Internally Balanced Structure:** A method for selecting minimal number of external FFs to form an internally balanced structure is as follows:

Step 1: separate separable primary input branches.

Step 2: select minimum number of external FFs to form a balanced structure for this circuit by using the above method [3].

Since internally balanced structures are usually considered wider than balanced structures, the external FFs for extracting the kernel circuit are ultimately fewer than for a balanced structure.

## 7 APPLICATION TO DESIGN FOR TESTABILITY BASED ON PARTIAL SCAN

### 7.1 Partial Scan Design

Full scan design can be used for design for testability allowing test generation based only on a combinational test generation algorithm. However, there is an overhead problem because all FFs are scan FFs. There are many partial scan design approaches [7], [8], [9], [10]. Since sequential circuits with internally balanced structure allow test generation with combinational test generation complexity, it is sufficient to perform a partial scan such that the circuit with exclusion of the scan FFs (kernel circuit) becomes an internally balanced structure. In the partial scan design with the kernel circuit constituting an internally

balanced structure, test simplification up to combinational level in the true sense can be achieved.

### 7.2 Experimental Results

We conducted comparative experiments for the cases without scan design, with full scan design, and with partial scan design, wherein the scan FFs were selected so as to have the kernel circuit as an internally balanced structure (using the technique described). For the experiments, we used a Sun4/10 Model 512 workstation and, as CAD software, we used the B-Chart input software for RTL circuit patterns (a product of Matsushita Electric Corporation). We also used AutoLogic synthesis software (Mentor Graphics) and TestGen automatic test generation software (SunRise). We generated various tests aimed at the two circuit examples, with the data path system organized using adders and multipliers, and, in particular, circuits resulting from design and logic synthesis starting at the register transfer level, circuits designed by full scan, and circuits based on internally balanced structure and modified using the partial scan technique (the technique described above). The external FFs shown in Table 1 are regarded in this technique as scan FFs. The items in Tables 2 and 3 have the following meanings:

Fault coverage: the ratio of the number of faults detected to the total number of faults,

Fault efficiency: the ratio of the number of faults detected plus the number of faults identified as redundant to the total number of faults,

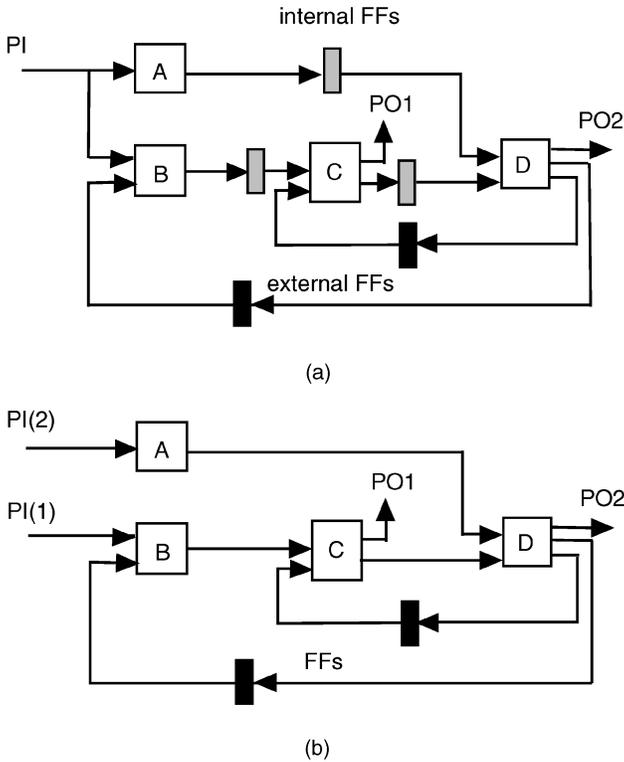


Fig. 20. (a) Sequential circuit S and (b) its transformed circuit  $S^R$ .

Number of test patterns: the number of test patterns for the kernel part,

Test sequence length: the length of test sequences for the entire circuit.

When compared to the case without scan design, both the full scan design and the partial scan design based on the proposed technique allow a fault efficiency close to 100 percent to be attained (thanks to the combinational test generation complexity). In addition, the test generation time can be significantly reduced. On the other hand, comparison of the full scan test with the proposed technique demonstrated that the test generation time is shorter for the full scan technique. The reason is that the test generation was made simpler at the cost of a larger number of scan FFs and more numerous inputs and outputs of the kernel circuit. The partial scan design based on the proposed technique consumes more time for test generation than the full scan design, but since it allows test generation based on the combinational test generation algorithm, the test generation can be completed in comparatively short time. Comparison of the test sequence length demonstrated that it was shorter in the case of the proposed technique than in the full scan design. More detailed discussion on this application and the experimental results was reported in [11] by Takasaki et al.

### 8 APPLICATION FOR TIME REDUCTION IN SEQUENTIAL TEST GENERATION

In a sequential circuit allowing test generation with combinational test generation complexity, the problem of test generation is reduced to the problem of test generation

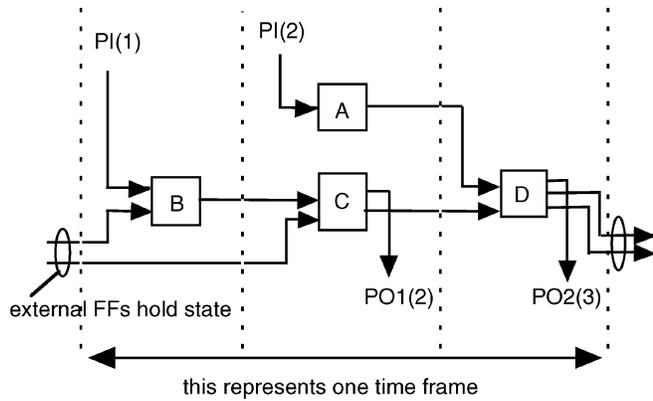


Fig. 21. One time frame in SR.

in an equivalent combinational circuit. In this section, we shall demonstrate a method that reduces the test generation time while applying this feature to sequential circuits in general.

We shall propose *circuit pseudotransformation* which changes a circuit under consideration into a different circuit whose test generation is easier than the original one, where the circuit is not changed physically but is just transformed tentatively only during test generation. The *software transformation* [12] is a circuit pseudotransformation based on retiming technique. We shall present a different circuit pseudotransformation based on internally balanced structure.

#### 8.1 Test Generation Technique

Step 1: A given sequential circuit S is divided into internal FFs and external FFs as shown in Fig. 19. During this operation, we select the minimum number of external FFs so that the kernel circuit (internal FFs and combinational circuit) would constitute an internally balanced structure.

Step 2: Upon separating primary inputs which are separable, the internal FFs are replaced by wires. The result is denoted by  $S^R$ .

Step 3: The test generation algorithm for sequential circuits is applied to  $S^R$ . Since the number of FFs in  $S^R$  is reduced as compared to the number of FFs in S, the test generation time is shorter.

Consider the sequential circuit S in Fig. 20a. As illustrated in the diagram, on dividing it into the internal FFs and external FFs, the kernel circuit has internally balanced structure. After separation of the separable primary inputs (PIs) and substituting wires for the internal

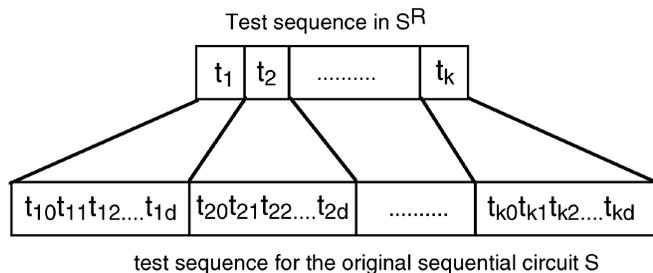


Fig. 22. Reverse transformation of the test sequence.

TABLE 4  
Circuit 1

	Fault coverage	Fault efficiency	Test sequence length in $S^R$	Test sequence length in S	Test generation time
conventional method	77.99%	93.04%	-----	200	3369 sec
proposed method	83.95%	98.45%	84	252	2162 sec

TABLE 5  
Circuit 2

	Fault coverage	Fault efficiency	Test sequence length in $S^R$	Test sequence length in S	Test generation time
conventional method	49.28%	65.67%	-----	59	31,815 sec
proposed method	63.69%	79.71%	61	183	17,025 sec

FFs, we have circuit  $S^R$  shown in Fig. 20b. The test sequence for this circuit  $S^R$  is obtained by applying the test generation algorithm for sequential circuits. Here, test generation is performed by regarding the kernel circuit (shown in Fig. 21) as a combinational circuit. Therefore, when the test sequence generated for  $S^R$  is applied to the original sequential circuit S, the state of the external FFs must be held during the time of signal propagation through the kernel circuit, i.e., during  $d + 1$  clock cycles. Hence, the test sequence for the original sequential circuit S can be obtained by expanding all the time frames of the test sequence obtained for  $S^R$  to the time frame  $d + 1$  (see Fig. 22).

## 8.2 Experimental Results

Test generation was performed for the two circuits with the data path system described in Section 7.2. After completing design and logic synthesis from the register transfer level, test generation was performed for the synthesized sequential circuit S and the sequential circuit  $S^R$  obtained by transformation of S in accordance with the proposed technique. Compared to the original circuit S, the sequential circuit  $S^R$  had fewer FF on account of the internal FFs, according to Table 1. The results are summarized in Tables 4 and 5. In the proposed technique, the test sequence consumed more time than in the conventional technique; however, it yielded better results in fault coverage, fault efficiency, and test generation time. More detailed discussion on this application and the experimental results was reported in [14] by Ohtake et al.

## 9 CONCLUSION

We have defined classes for sequential circuits allowing test generation with combinational test generation complexity and have identified their characteristics. The acyclic structures do not exhibit these characteristics. We introduced a new class of internally balanced structures as a class that exhibits these characteristics. The FSMs that can be realized with acyclic structures can be also realized with

internally balanced structures. Further, we introduced a new definition of test generation possibility with combinational test generation complexity. In this paper, we additionally studied applications to design for testability based on the partial scan and to test generation time reduction for sequential circuits in general, using characteristics of the internally balanced structures. The experimental results showed the effectiveness of this approach.

## ACKNOWLEDGMENTS

The author would like to thank Toshimitsu Masuzawa, Michiko Inoue, Satoshi Ohtake, and Tomoya Takasaki of the Nara Institute of Science and Technology, and Tomoo Inoue of Hiroshima City University for their helpful discussion. This work was supported in part by the Ministry of Education, Science, Sports, and Culture, Japan under the Grant-in-Aid for Scientific Research B(2) (No. 09480054).

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