



Sequential Circuits with Combinational Test Generation Complexity under Single-Fault Assumption

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Abstract. We show that the test generation problem for *all* single stuck-at faults in sequential circuits with internally balanced structures can be reduced into the test generation problem for single stuck-at faults in combinational circuits. In our previous work, we introduced *internally balanced structures* as a class of sequential circuits with the combinational test generation complexity. However, single stuck-at faults on some primary inputs, called *separable primary inputs*, corresponded to multiple stuck-at faults in a transformed combinational circuit. In this paper, we resolve this problem. We show how to generate a test sequence and identify undetectability for single stuck-at faults on separable primary inputs.

Keywords: test generation, combinational circuit, sequential circuit, balanced structure, internally balanced structure

1. Introduction

Test generation for sequential circuits is, in general, a difficult and intractable task which may be unsolvable within reasonable amount of time for a large-scale circuit [1, 5]. When all the flip-flops of a circuit are

replaced with scan flip-flops (*full scan design*), all the scan flip-flops are treated as equivalents to external I/O terminals and hence the test generation can be performed for the remaining circuit (called the “kernel circuit”) with the exclusion of all flip-flops, i.e., for the combinational part of the sequential circuit. Therefore, the full scan design method can reduce the test generation problem for a sequential circuit to the test

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generation problem for a combinational circuit. We shall consider only stuck-at faults in this paper, and refer to *stuck-at faults* to hereafter just as *faults*.

To reduce area and delay overhead while preserving the above good feature of the full scan design, a class of sequential circuits that allows test generation with combinational test generation algorithms has been investigated [2, 6–9]. *Balanced structures* [8] are one class of circuit structures with this feature. A sequential circuit is a balanced structure if it is acyclic and all paths between any pair of primary input and primary output have the same number of flip-flops. For a balanced sequential circuit, test generation problem can be reduced into the test generation problem for a combinational circuit obtained by replacing all flip-flops with wires. In this transformation, all *single* faults on a balanced circuit correspond to *single* faults on the transformed combinational circuit. In [2], a sub-class of balanced structure called *strongly balanced structures* is introduced to reduce test application time. In [7], a balanced structure is considered at register-transfer level. At this level, the functional behavior of the combinational logic such as “switch” can be considered, and *switched balanced structures* are introduced as a larger class of the balanced structures. For an acyclic structure, test generation method that uses combinational test generation algorithm for a *time expansion model* is proposed [9]. Although this model allows test generation with combinational test generation algorithm, it includes multiple copies of the combinational blocks of the original sequential circuits. Therefore, the transformed circuits is much larger than the original circuit, and moreover, a single fault in the original circuit may correspond to a *multiple* fault in the transformed circuit. In general, the single stuck-at faults can be used to model other type of faults (see [1], pp.111, 112), and hence multiple stuck-at faults can be modeled by single stuck-at faults. However, the approach requires additional circuitry for each fault to the circuit, and therefore, the size of the circuit under test is enlarged.

In [6], we introduced a new class of sequential circuits with combinational test generation complexity called *internally balanced* structure. This class is larger than the class of balanced structures. When considering realization possibility of finite state machines (FSMs), it is shown that $\{\text{FSMs which can be realized as a sequential circuit of acyclic structure}\} = \{\text{FSMs which can be realized as a sequential circuit of internally balanced structure}\} \supset \{\text{FSMs which can be realized as a sequential circuit of balanced structure}\}$. We reduced

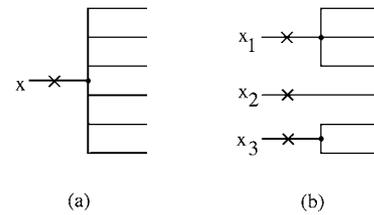


Fig. 1. Correspondence of faults: (a) A separable primary input in S , (b) separated primary inputs in C .

the test generation problem for faults in a circuit S with an internally balanced structure into the test generation problem for faults in a combinational circuit C where some primary inputs with fanout branches in S are separated into two or more primary inputs according to some partition of the fanout branches. We call such primary inputs in S *separable primary inputs*. Any part in S except for the separable primary inputs is not replicated in C . Therefore, each single fault on a separable primary input in S corresponds to a *multiple* fault on the separated primary inputs in C , while the other single faults in S correspond to *single* faults in C . Fig. 1 shows an example. The original circuit S has a separable primary input x (Fig. 1(a)) separated into three primary inputs x_1, x_2, x_3 in the transformed circuit C (Fig. 1(b)). In such transformation, the fault on x in S corresponds to a multiple fault on x_1, x_2, x_3 in C .

In this paper, we desire to generate test sequences for single faults on the separable primary inputs without any modification of S or C . The separable primary inputs have fanout branches, and we consider the relation between a multiple faults on all the fanout branches and single faults on the fanout branches. There are many works on fanout faults or multiple faults including [3, 4, 10].

First, we show that test sequences corresponding to test patterns for single faults on separated primary inputs do not always detect faults on the separable primary inputs. This means that even if we can find test patterns for all detectable faults on the primary inputs in C separated from a primary input x in S , test sequences corresponding to these test patterns may not detect the fault on x though it is detectable.

Next, we present how to find test sequences for single faults on the separable primary inputs. We show that we can get a test sequence for a single stuck-at- v fault on a separable primary input directly from a test pattern for a single stuck-at- v fault on one of the separated primary inputs. Finally, we show that a single

stuck-at- v fault on a separable primary input is undetectable if all single stuck-at- v faults on the separated primary inputs are undetectable. In this way, we reduce the test generation problem for single faults in circuits with internally balanced structures into the test generation problem for *single* faults in combinational circuits. Moreover, the size of the transformed combinational circuit is not larger than the original sequential circuit.

The rest of this paper is organized as follows. In Section 2, the internally balanced structure and some notations are provided. We show that faults on the separable primary inputs may not be detected by test sequences for the separated primary inputs, and show how to generate complete test sequences and identify undetectable faults in Section 3. Section 4 concludes the paper.

2. Preliminaries

First, we briefly define the internally balanced structure [6]. For simplicity, we shall limit flip-flops (referred to hereafter as FFs) to DFFs. Another kind of FFs can be handled similarly.

The number of FFs included in a path is called a sequential depth of the path. The largest sequential depth over the paths from the primary inputs of a sequential circuit to a primary output is regarded as a sequential depth of the primary output. The largest sequential depth over the primary outputs is regarded as a sequential depth of the sequential circuit. In this paper, we treat only acyclic sequential circuits, and therefore, we can find the sequential depth of any primary output and the sequential depth of the sequential circuit. Suppose x is a primary input, and y_i and y_j are fanout branches of x . If there is no primary output that can be reached from y_i and y_j over equal depth paths, then y_i and y_j are called *separable*.

A partition Π on a set A is a collection of disjoint subsets whose set union is A . The disjoint subsets are called the *blocks* of Π . A partition Π_1 on A is said to be “smaller than or equal to” Π_2 on A if and only if each pair of elements which are in a common block of Π_1 are also in a common block of Π_2 .

Extended Combinational Transformation: A transformation based on the following two operations with a sequential circuit S of acyclic structure is called an extended combinational transformation (C^* -transformation), and the resulting combinational circuit is denoted by $C^*(S)$.

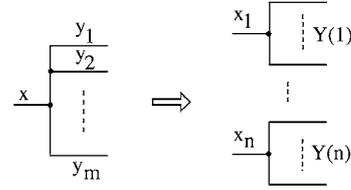


Fig. 2. Primary input separation.

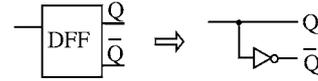


Fig. 3. Deletion of flip-flops.

1. *Separation of primary inputs:* For each primary input x with fanout branches, *separate* it as follows. Let Y denote a set of the fanout branches of a primary input. Let us obtain the smallest partition Π of Y which satisfies the following statement: If branches y_a and y_b belong to different blocks $Y(i), Y(j)$ of partition Π ($y_a \in Y(i), y_b \in Y(j), Y(i) \neq Y(j)$) then y_a and y_b are separable. As shown in Fig. 2, each partitioned block $Y(i)$ is provided with a new primary input x_i separated from the original primary input x .
2. *C^* -transformation:* Replace each FF by a wire (for the case of negative FF output, a NOT gate is added, see Fig. 3).

Note that we can uniquely obtain the smallest partition Π for each primary input as connected components of a graph such that the vertices are the fanout branches and an edge exists iff two fanout branches are not separable. In this way, for a given acyclic circuit S , the resulting circuit from the operation (1) of the C^* -transformation and the resulting circuit $C^*(S)$ from the C^* -transformation are uniquely determined.

Balanced Structure [6]: For any pair of primary input and primary output in an acyclic circuit S , if the sequential depths of all paths connecting these two points are equal, then S is regarded as a *balanced structure*.

Internally Balanced Structure [4]: An acyclic circuit S is regarded as an *internally balanced structure* if the circuit resulting from the operation (1) of the C^* -transformation on S is a balanced structure.

The circuit shown in Fig. 4(a) is an internally balanced structure but is not a balanced structure where

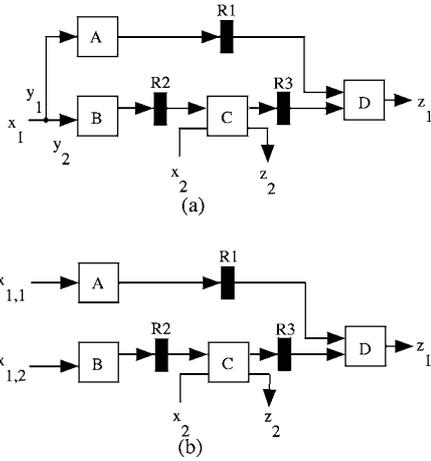


Fig. 4. (a) Example of internally balanced structure, (b) Circuit resulting from the operation (1) of the C^* -transformation.

A, B, C, D are blocks of combinational logics and $R1, R2, R3$ are registers (collections of FFs). Fig. 4(b) shows the circuit resulting from the operation (1) of the C^* -transformation on the circuit in Fig. 4(a), where a primary input x_1 is separated into two primary inputs $x_{1,1}$ and $x_{1,2}$, and the circuit in Fig. 4(b) is a balanced structure. Therefore, the circuit in Fig. 4(a) is an internally balanced structure. Clearly, if the circuit is balanced structure then it is also internally balanced structure. The relation among the structures is as follows: {sequential circuits with acyclic structure} \supset {sequential circuits with internally balanced structure} \supset {sequential circuits with balanced structure}.

Let S be a circuit with an internally balanced structure. We consider a transformation of a test pattern for $C^*(S)$ into a test sequence T for S . First, we define a transformation of a test sequence T for S into a test pattern for $C^*(S)$. The transformation of a test pattern into a test sequence is defined as the reverse function.

Let z be a primary output in S such that T propagates a fault effect to a primary output z in time frame τ . Let $T_c(T, S, z, \tau)$ be a test pattern for $C^*(S)$ which is transformed from a test sequence T for S as follows. Assume that the length of T and the time frame τ are both more than the sequential depth of z . If there is no path from a primary input x to z in $C^*(S)$, we consider the value of x as *don't care*, otherwise, the following two cases exist.

1. Case where x is a primary input in S and is not separated in $C^*(S)$: The sequential depth d of any

path from x to z is uniquely determined. The value of x in $T_c(T, S, z, \tau)$ is the value of x of T in time frame $\tau - d$.

2. Case where x is a primary input in S and is separated in $C^*(S)$: Assume that the primary input x in S is separated to obtain the primary inputs x_1, x_2, \dots, x_n in $C^*(S)$. Since S is an internally balanced structure, any path from $x_j (j = 1, 2, \dots, n)$ to z has unique sequential depth d_j . The value of $x_j (j = 1, 2, \dots, n)$ of test pattern $T_c(T, S, z, \tau)$ is the value of x of T in time frames $\tau - d_j (j = 1, 2, \dots, n)$.

Now we consider the reverse transformation. Let t be a test pattern for $C^*(S)$ that propagates a fault effect to a primary output z , and let d be the sequential depth of z . We can define a test sequence that propagates a fault effect in time frame $d + 1$. Since all the sequential depths $d_j (j = 1, 2, \dots, n)$ in the second case are different from each other, the values of $x_j (j = 1, 2, \dots, n)$ correspond into the values of x of the test sequence in distinct time frames. Therefore, we can define a test sequence T from a test pattern t satisfying $t = T_c(T, S, z, d + 1)$.

Example 1. Fig. 5(a) shows a sequential circuit S with an internally balanced structure where a primary input x_2 is separable. We can obtain a circuit $C^*(S)$ in Fig. 5(b) where x_2 is separated into $x_{2,1}$ and $x_{2,2}$. For S , input sequence $T = (000, 101)$ is a test sequence detecting the stuck-at-1 fault on y_1 which

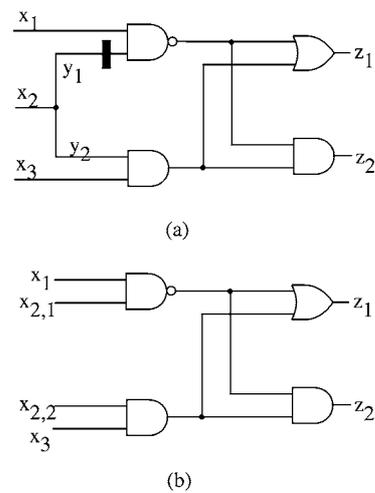


Fig. 5. (a) Internally balanced structure S , (b) Combinational equivalent $C^*(S)$.

propagates a fault effect to a primary output z_1 in time frame 2. This sequence is transformed to a test pattern $t = T_c(T, S, z_1, 2) = ((x_1 = 1, x_{2,1} = 0, x_{2,2} = 0, x_3 = 1))$ for the stuck-at-1 fault on $x_{2,1}$ in $C^*(S)$. On the other hand, any test sequence T satisfying $(1001) = T_c(T, S, z_1, 2)$ detects the stuck-at-1 fault on y_1 in S . Since the sequential depth of a path from $x_{2,1}$ to z_1 is 1 and the sequential depth of the other path to z_1 are 0, the value of $x_{2,1}$ corresponds to the value of x_2 in time frame $2 - 1 = 1$ and the other values correspond to the values in time frame $2 - 0 = 2$. Therefore an input sequence $(-0-, 101)$ is such a sequence where ‘-’ means don’t care.

Possibility of Test Generation with Combinational Test Generation Complexity

In [6], we defined the possibility of test generation with combinational test generation complexity as follows: If the test generation problem for a sequential circuit S can be reduced to the test generation problem of C^* -transformed combinational circuit $C^*(S)$, S allows test generation with combinational test generation complexity. Such a sequential circuits is called a *sequential circuit allowing test generation with combinational test generation complexity*, or, simply, a *sequential circuit with combinational test generation complexity*. We showed that the test generation problem for a sequential circuits S with internally balanced structure can be reduced to the test generation problem for a combinational circuit $C^*(S)$.

This is the extension of the definition of the possibility of test generation with combinational test generation complexity in [8], where they use C -transformaion as the transformaiton to combinational circuits. We extended the defintioin by introducing C^* -transformaion. In [6], we further extended the definition to more general form, where we require the time complexities of the transfromation and test generation of the transformed combinational circuit are less than the time complexity of the test generation of the original sequential circuit.

Theorem 1 ([4]). *If a sequential circuit S is an internally balanced structure, S allows test generation with combinational test generation complexity.*

However, each fault on a separable primary input x in S corresponds to a multiple fault on all the separated primary inputs of x in $C^*(S)$. On the other hand, any other single fault f in S corresponds to a single fault f'

on the same line in $C^*(S)$, and a test pattern t detects f' iff any test sequence satisfying $t = T_c(T, S, z, d + 1)$ detects f in S where t propagates a fault effect to a primary output z with a sequential depth d .

3. Detection of Separable Primary Input Faults

In this section, we consider whether the test generation problem for *single* faults in a sequential circuit S with internally balanced structures can be reduced to the test generation problem for *single* faults in a combinational circuit $C^*(S)$. Since the test generation problem for all single faults except on separable primary inputs in S can be reduced into the test generation problem for single faults in $C^*(S)$, we only consider single faults on separable primary inputs.

We consider whether the test generation problem for a single fault on a separable primary input x in S can be reduced into the test generation problem for single faults on primary inputs separated from x in $C^*(S)$. First, we show that test sequences corresponding to test patterns for single faults on separated primary inputs do not always detect faults on the separable primary inputs.

Theorem 2. *Let S be a sequential circuit S with internally balanced structure. The following statement does not hold: For any primary input x in S which is separated into x_1, x_i, \dots, x_n in $C^*(S)$, if $\{t_1, t_2, \dots, t_k\} \neq \emptyset$ is a complete test set for the single stuck-at- v faults on x_1, x_i, \dots, x_n in $C^*(S)$ then there exists a test pattern $t \in \{t_1, t_2, \dots, t_k\}$ such that any test sequences T satisfying $t = T_c(T, S, z, d + 1)$ detects a stuck-at- v fault on x in S where t propagates a fault effect to a primary output z and d is a sequential depth of z in S .*

Proof: Consider the circuits in Fig. 5 again. To prove the theorem, it is sufficient to show that, for each $x_{2,j}$ ($j = 1, 2$), there is a test pattern t such that it detects the single stuck-at- v fault on $x_{2,j}$ and that some sequence T satisfying $t = T_c(T, S, z, d + 1)$ cannot detect the stuck-at- v fault on x_2 , where t propagates a fault effect to a primary output z and d is the sequential depth of z in S .

Now, we show such test patterns for stuck-at-1 faults on $x_{2,1}$ and $x_{2,2}$. The test pattern $t = (x_1 = 1, x_{2,1} = 0, x_{2,2} = 0, x_3 = 1)$ can detect both stuck-at-1 faults on $x_{2,1}$ and $x_{2,2}$ in $C^*(S)$. It propagates D to z_1 for the fault on $x_{2,1}$ and \bar{D} to z_2 for the fault on $x_{2,2}$. Both sequential depths of z_1 and z_2 are 1, and the sequence

$T = (000, 101)$ satisfies $t = T_c(T, S, z_1, 2)$ and $t = T_c(T, S, z_2, 2)$ but does not detect the stuck-at-1 fault on x_2 . ■

Although Theorem 2 means that we cannot find a test sequence for a fault on a separable primary input directly from test patterns for separated primary inputs, we can find such a test sequence which detects a fault on a separable primary input. For an input pattern $t = (v_1, v_2, \dots, v_m)$ for a combinational circuit with primary inputs x_1, x_2, \dots, x_m , let $t[x_i := w_i, x_j := w_j, \dots]$ denote the input pattern obtained from replacing the values of x_i, x_j, \dots with the values w_i, w_j, \dots .

In [6], it is shown that a single stuck-at- v fault on a separable primary input x in a sequential circuit S with internally balanced structure is detectable iff the multiple stuck-at- v fault on all the separated primary inputs in $C^*(S)$ is detectable. The following theorems consider a multiple fault on some of primary inputs in a combinational circuit.

Theorem 3. *Let x_1, x_2, \dots, x_m be a subset of primary inputs in a combinational circuit C . For any $j \in \{1, 2, \dots, m\}$, if t is a test pattern for a single stuck-at- v fault f_j on some x_j in C , then a multiple stuck-at- v fault f on x_1, x_2, \dots, x_n can be detected by t or $t[x_j := v]$.*

Proof: Let z be a primary output to which t propagates a fault effect, and let $F(x_1, x_2, \dots, x_n, X)$ be a function of z where X is a list of primary inputs other than x_1, x_2, \dots, x_n . Since t detects f_j , the value of x_j in t must be \bar{v} and $F(t) \neq F(t[x_j := v])$ holds. Let F_f denote the value of z in C with the fault f .

1. Case of $F(t) \neq F(t[x_1 := v, \dots, x_n := v])$: In this case, $F_f(t) = F(t[x_1 := v, \dots, x_n := v]) \neq F(t)$ holds. Therefore, f can be detected by t .
2. Case of $F(t) = F(t[x_1 := v, \dots, x_n := v])$: $F_f(t[x_j := v]) = F(t[x_1 := v, \dots, x_n := v]) = F(t) \neq F(t[x_j := v])$. Therefore, f can be detected by $t[x_j := v]$. ■

Let $\mathcal{T}_{S,x,v}$ ($\mathcal{T}_{C,x,v}$) denote a set of test sequences (test patterns) that detect a stuck-at- v on a line x in a sequential circuit S (a combinational circuit C).

Theorem 4. *Let x_1, x_2, \dots, x_m be primary inputs in a combinational circuit C . If $\bigcup_{1 \leq j \leq m} \mathcal{T}_{C,x_j,v} = \emptyset$ holds*

then the multiple stuck-at- v fault f on x_1, x_2, \dots, x_m in C is undetectable.

Proof: We prove the theorem by contradiction. Assume $\bigcup_{1 \leq j \leq m} \mathcal{T}_{C,x_j,v} = \emptyset$ but there is a test pattern t that detects f . Let z be a primary output to which t propagates a fault effect. Let F be a function of z in C . Since there is no test pattern for stuck-at- v fault on any x_j , $F(t') = F(t'[x_j := 0]) = F(t'[x_j := 1]) = F(t'[x_j := v])$ holds for any x_j and any input pattern t' .

Since t is a test pattern for f , $F(t) \neq F(t[x_1 := v, \dots, x_n := v])$ holds. However, the following also holds.

$$\begin{aligned} & F(t) \\ &= F(t[x_1 := v]) \\ &= F(t[x_1 := v, x_2 := v]) \\ &\dots \\ &= F(t[x_1 := v, \dots, x_n := v]) \end{aligned}$$

The contradiction occurs. ■

In [6], it is shown that a single stuck-at- v fault on x in S is detectable iff the multiple stuck-at- v fault on x_1, x_2, \dots, x_n in $C^*(S)$ is detectable. Therefore, Theorems 3 and 4 imply the following corollaries.

Corollary 5. *Let S be a sequential circuit with internally balanced structure, where a primary input x in S is separated into x_1, x_2, \dots, x_n in $C^*(S)$. If t is a test pattern for a single stuck-at- v fault f_j on some x_j in $C^*(S)$ ($j = 1, 2, \dots, n$), then a single stuck-at- v fault f on x in S can be detected by any T satisfying $t = T_c(T, S, z, d)$ or any T' satisfying $t[x_j := v] = T_c(T', S, z, d)$ where z is the primary output to which t propagates a fault effect and d is the sequential depth of z in S .*

Corollary 5 implies that $\bigcup_{1 \leq j \leq n} \mathcal{T}_{C^*(S),x_j,v} \neq \emptyset \Rightarrow \mathcal{T}_{S,x,v} \neq \emptyset$ holds.

Corollary 6. *Let S be a circuit with an internally balanced structure, where a primary input x is separated into x_1, x_2, \dots, x_n in $C^*(S)$. Then, $\bigcup_{1 \leq j \leq n} \mathcal{T}_{C^*(S),x_j,v} = \emptyset \Rightarrow \mathcal{T}_{S,x,v} = \emptyset$ holds.*

Example 2. Now, we consider the sequential circuit S in Fig. 5(a) again. $t = (x_1 = 1, x_{2,1} = 0, x_{2,2} = 0, x_3 = 1)$ can detect the stuck-at-1 fault on $x_{2,1}$ in $C^*(S)$. The test pattern t propagates D to z_1 which sequential depth is 1. However, some sequence T satisfying

$t = T_c(T, S, z_1, 2)$ ($T = 000, 101$ for example) does not detect the stuck-at-1 fault on x_2 . In this case, any sequence T' satisfying $t[x_{2,1} := 1] = T_c(T', S, z_1, 2)$, i.e., $T' = (-1-, 101)$, can detect the stuck-at-1 fault on x_2 .

Using the result in [6] and Corollaries 5 and 6, we can generate a test sequence for single faults in an internally balanced circuit S using a test generation algorithm for single faults in a combinational circuit $C^*(S)$. The procedure to generate a test sequence is as follows.

Test Generation Procedure

1. Transform S into a combinational circuit $C^*(S)$.
2. Generate test patterns for all single faults in $C^*(S)$ using a combinational test generation algorithm.
3. For all faults except on the separated primary inputs in C . Transform each test pattern t into a test sequence T satisfying $t = T_c(T, S, z, d)$ where t propagates a fault effect to a primary output z and d is the sequential depth of z in S . If a fault f in $C^*(S)$ is identified as undetectable, identify the corresponding fault in S as undetectable. Concatenate all obtained test sequences. Let \mathcal{T} be a concatenated sequence.
4. For each stuck-at- v fault on each separable primary input x in S , if some primary input x_j separated from x has a test pattern t for a stuck-at- v fault, then append a test sequence T satisfying $t = T_c(T, S, z, d)$ and a test sequence T' satisfying $t[x_j := v] = T_c(T', S, z, d)$ to \mathcal{T} where z is the primary output to which t propagates a fault effect and d is the sequential depth of z in S . Otherwise, identify a stuck-at- v fault on x as undetectable.

If a complete test generation algorithm for combinational circuits is available, the above procedure provides complete test sequence \mathcal{T} for the internally balanced circuit S . Note that the 4th step in the above procedure may add two test sequences for one single fault. Theorem 3 guarantees that one of the two sequences can detect the fault. Therefore, we can delete one of them from \mathcal{T} using a fault simulator to reduce the length of a test sequence.

4. Conclusion

In this paper, we considered the test generation problem for the single stuck-at- v faults on the separable primary

inputs of a sequential circuit with an internally balanced structure. We first showed that test sequences corresponding to test patterns for single stuck-at- v faults on the separated primary inputs x_1, x_2, \dots, x_n cannot always detect the single stuck-at- v fault on x . However, we showed that the single stuck-at- v fault on x can be detected if one of the stuck-at- v faults on the separated primary inputs is detected. We presented how to find a test sequence for the fault on x using a test pattern for any of the separated primary inputs. We also showed that if any single stuck-at- v fault on the separated primary inputs is undetectable then the single stuck-at- v fault on x is also undetectable. As a result, the test generation problem for single faults on separable primary inputs in a sequential circuit with an internally balanced structure can be reduced to the test generation problem for single faults in a combinational circuit.

In [6], it is shown that the test generation problem for single faults on all lines except for the separable primary inputs of a sequential circuit with an internally balanced structure can be reduced to the test generation problem for single faults in a combinational circuit. Moreover, the proposed transformation obtains a combinational circuit which is not larger than the original sequential circuit. From the result in this paper, we conclude that the test generation problem for *all* single faults in a sequential circuit with an internally balanced structure can be reduced to the test generation problem for single faults in a combinational circuit that is not larger than the original sequential circuit. We proposed the test generation procedure for internally balanced circuits. This procedure guarantees 100% fault efficiency if a complete test generation algorithm for single stuck-at faults in combinational circuits is available.

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